



COSIC

Higher-Order Threshold Implementations

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TWENTE.

Higher-Order Threshold Implementations

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In a nutshell:

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- A countermeasure against Higher-Order Differential Power Analysis (HO-DPA)

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- A countermeasure against Higher-Order Differential Power Analysis (HO-DPA)
- Ideas from secret sharing and multi-party computation
- Can be applied to any algorithm
- Independent of technology, library, etc.
- Efficient
- Application to KATAN-32

Background

Differential Power Analysis & Its Countermeasures

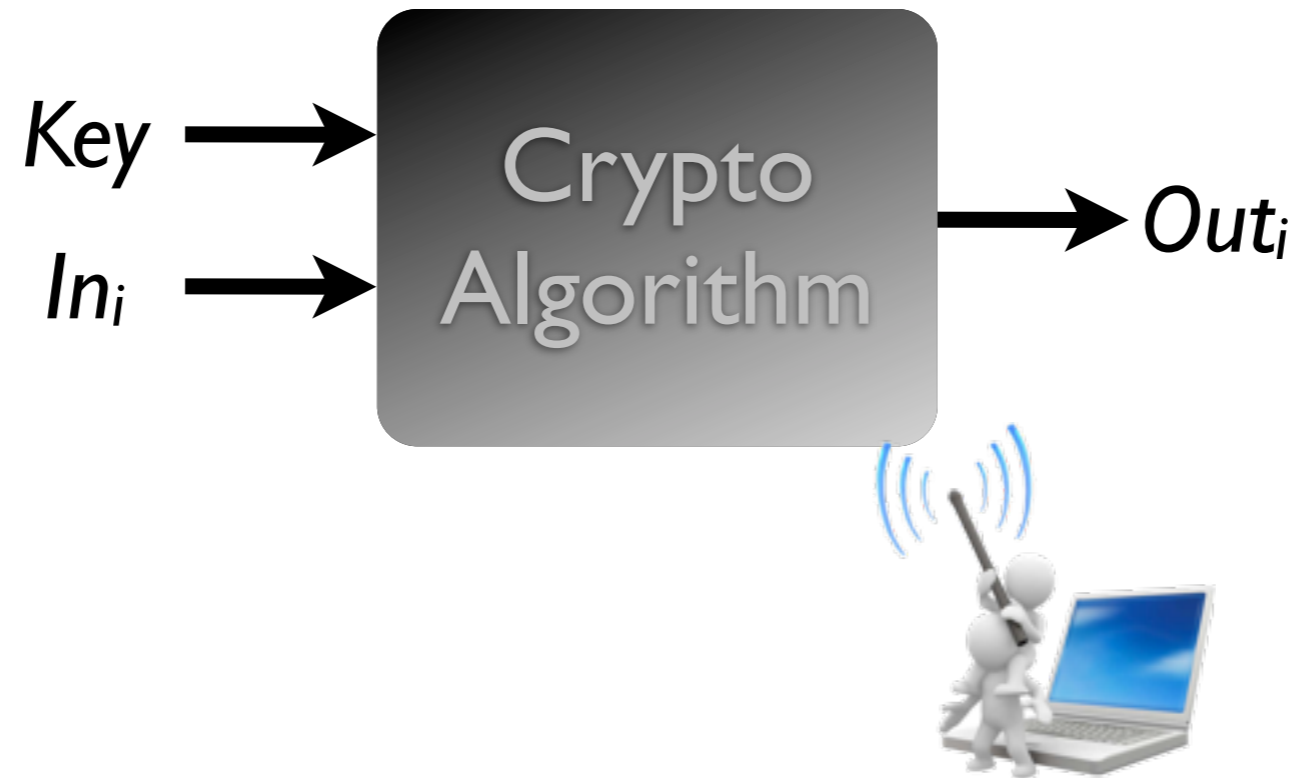
Background - DPA



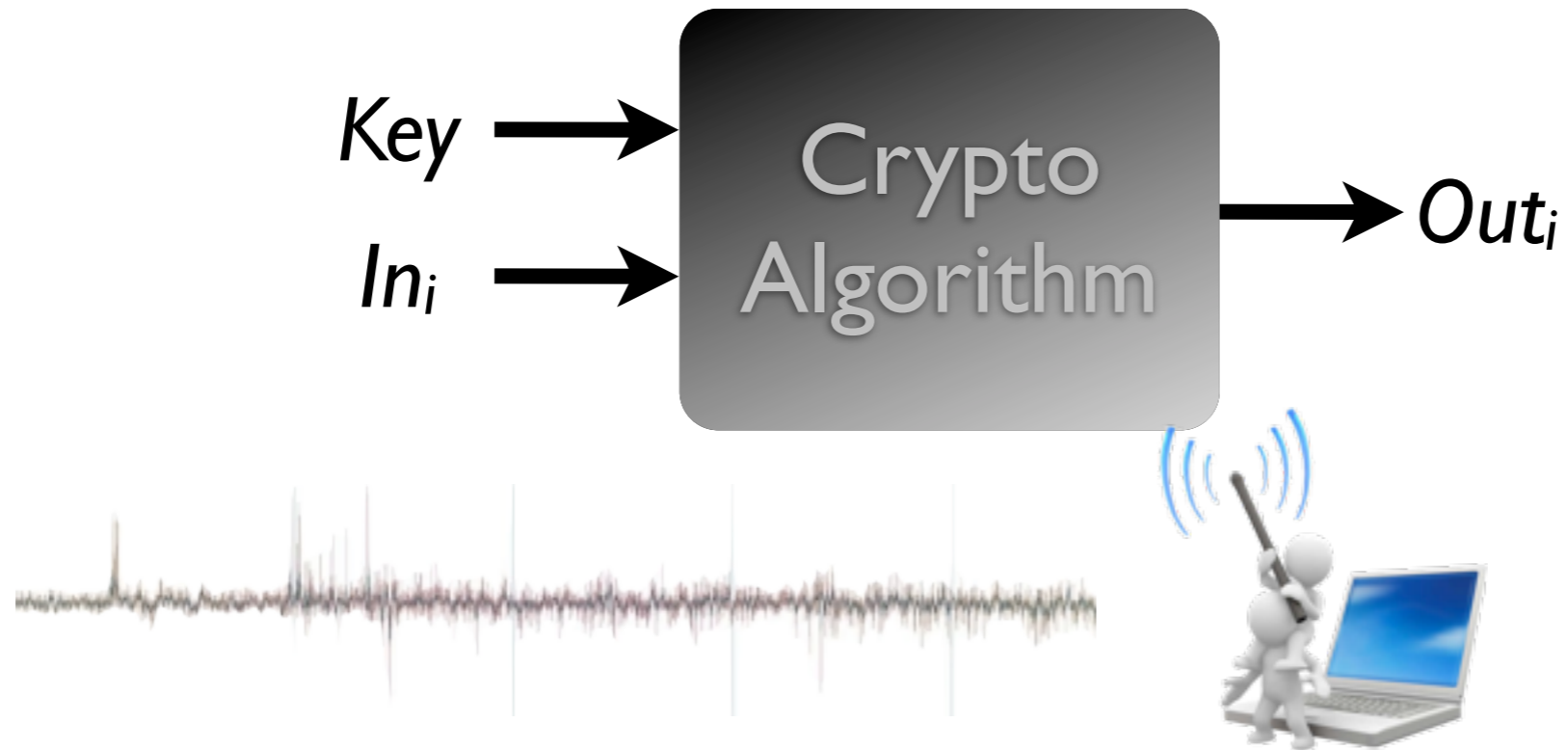
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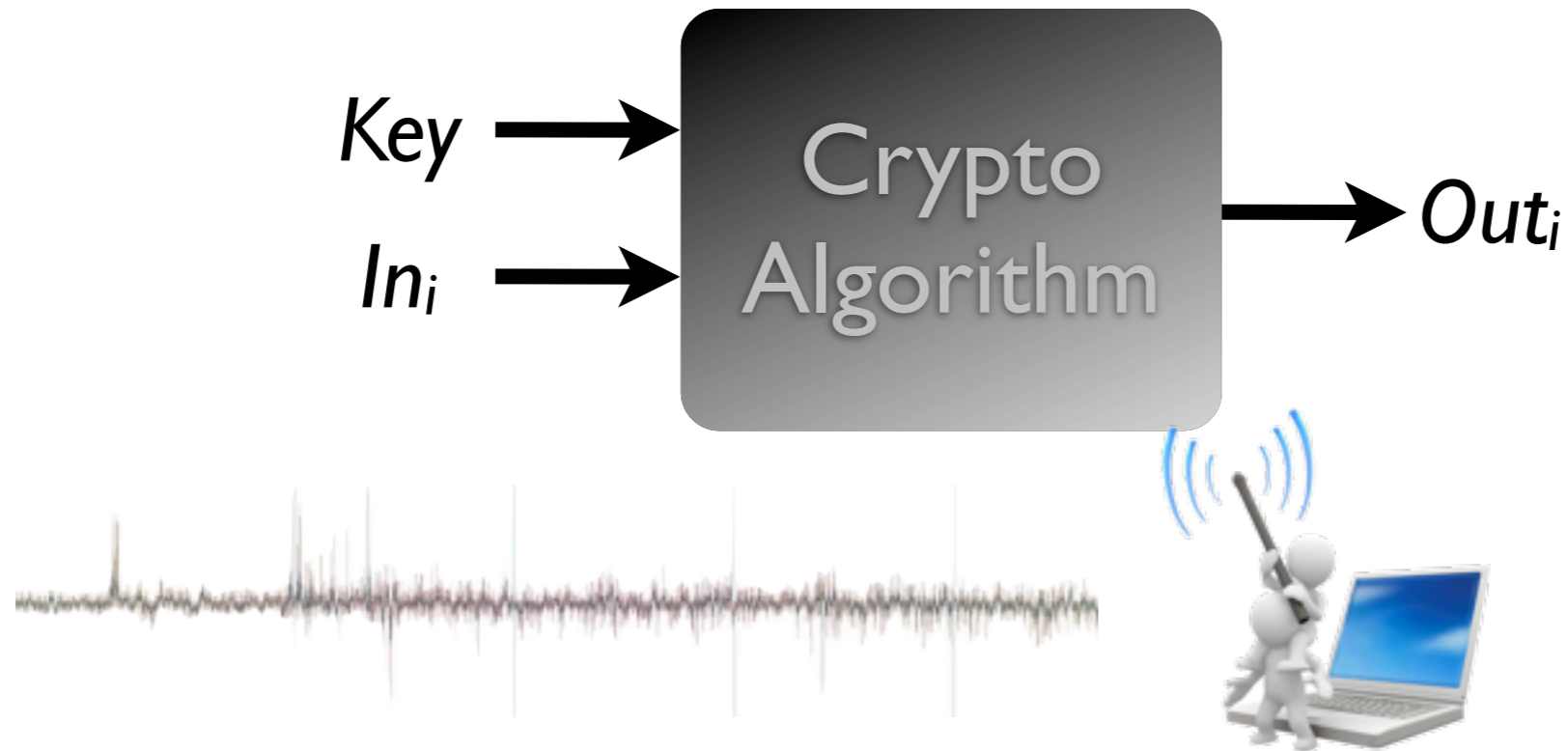
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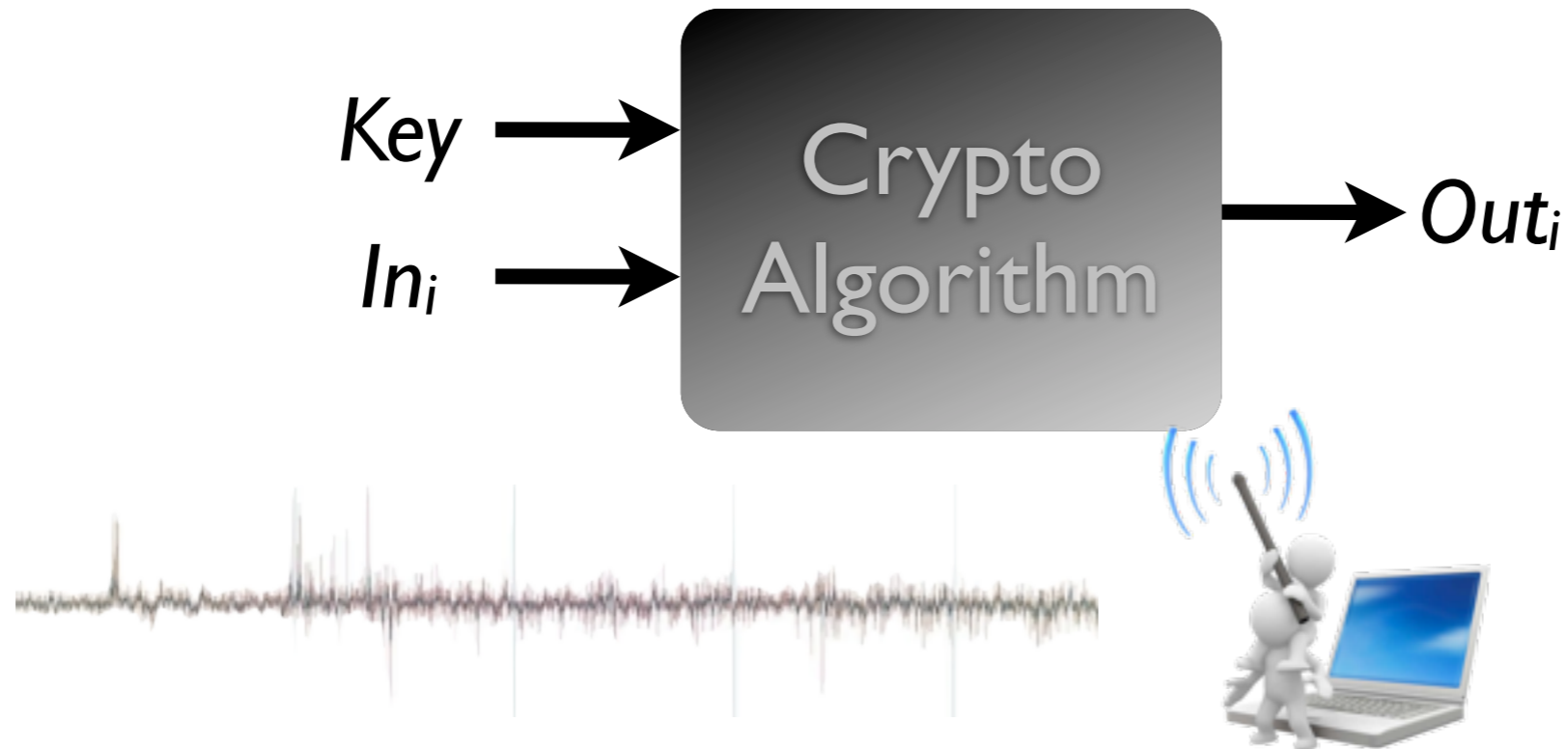


Background - DPA



DPA focuses on finding the secret using the relation between

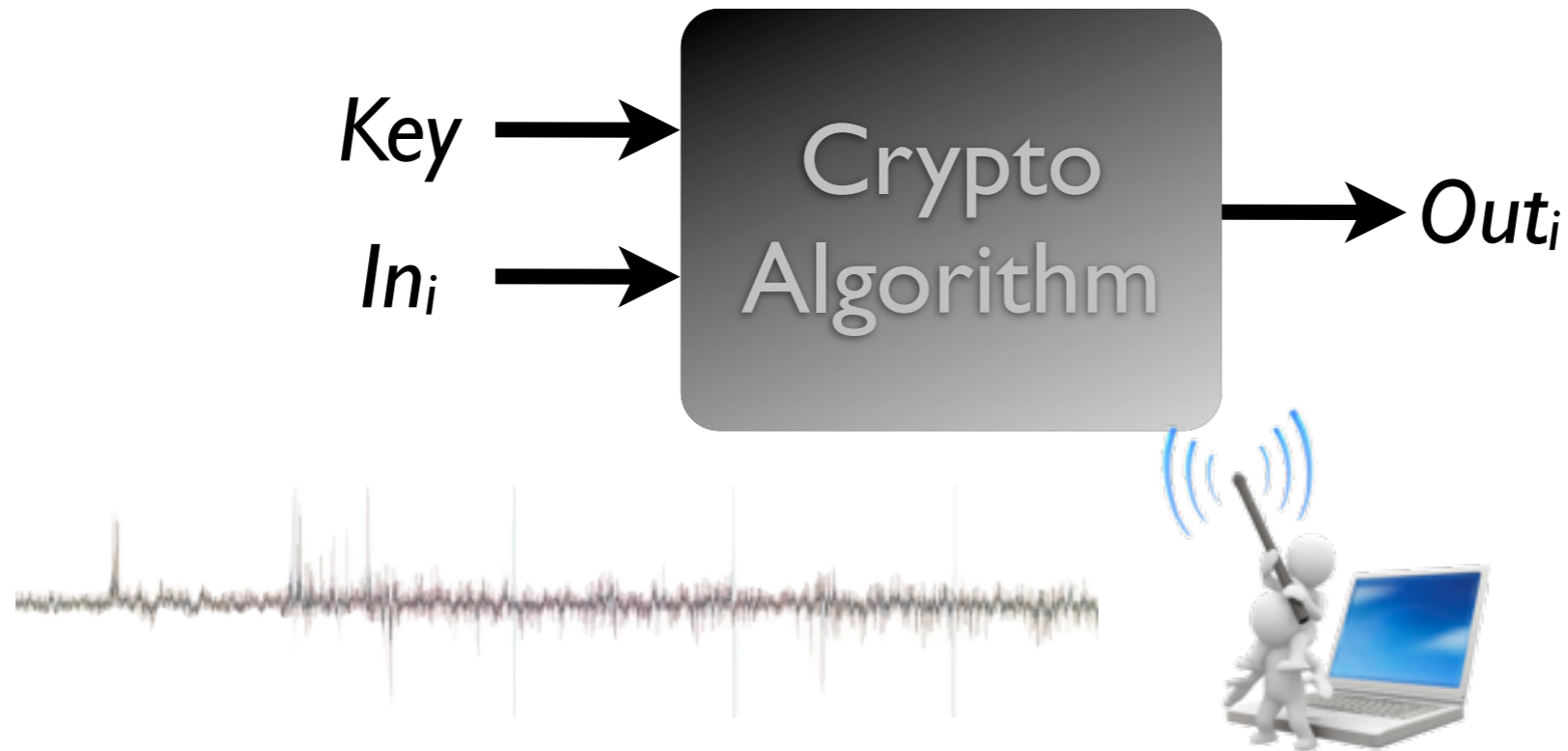
Background - DPA



DPA focuses on finding the secret using the relation between

- Instantaneous power consumption

Background - DPA



DPA focuses on finding the secret using the relation between

- Instantaneous power consumption
- And intermediate results of the algorithm

Background - DPA Countermeasures



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Countermeasure can be

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Countermeasure can be

- Limiting the usage of key

Background - DPA Countermeasures



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- Decreasing the SNR

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- Decreasing the SNR
- Breaking the relation between the trace and (In_i, Out_i)

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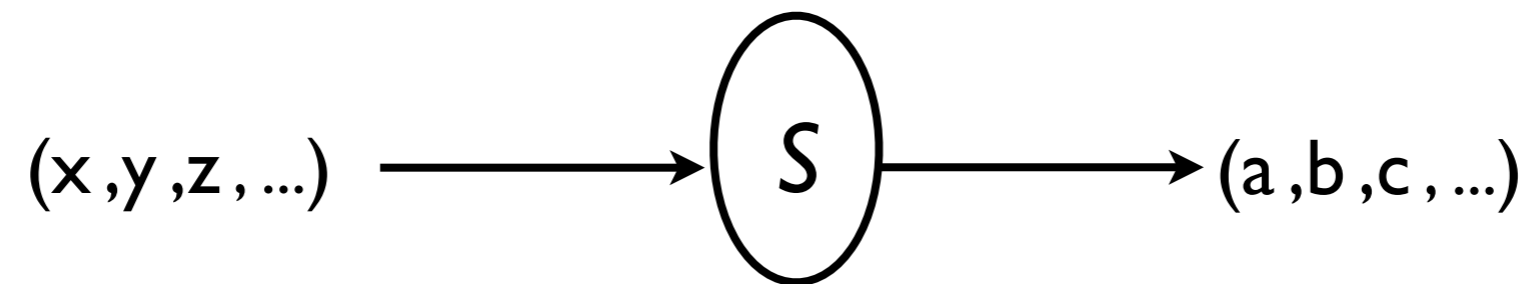


Countermeasure can be

- Limiting the usage of key
- Decreasing the SNR
- Breaking the relation between the trace and (In_i, Out_i)

e.g. Masking

Background - Boolean Masking



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(x_1, y_1, z_1, \dots)

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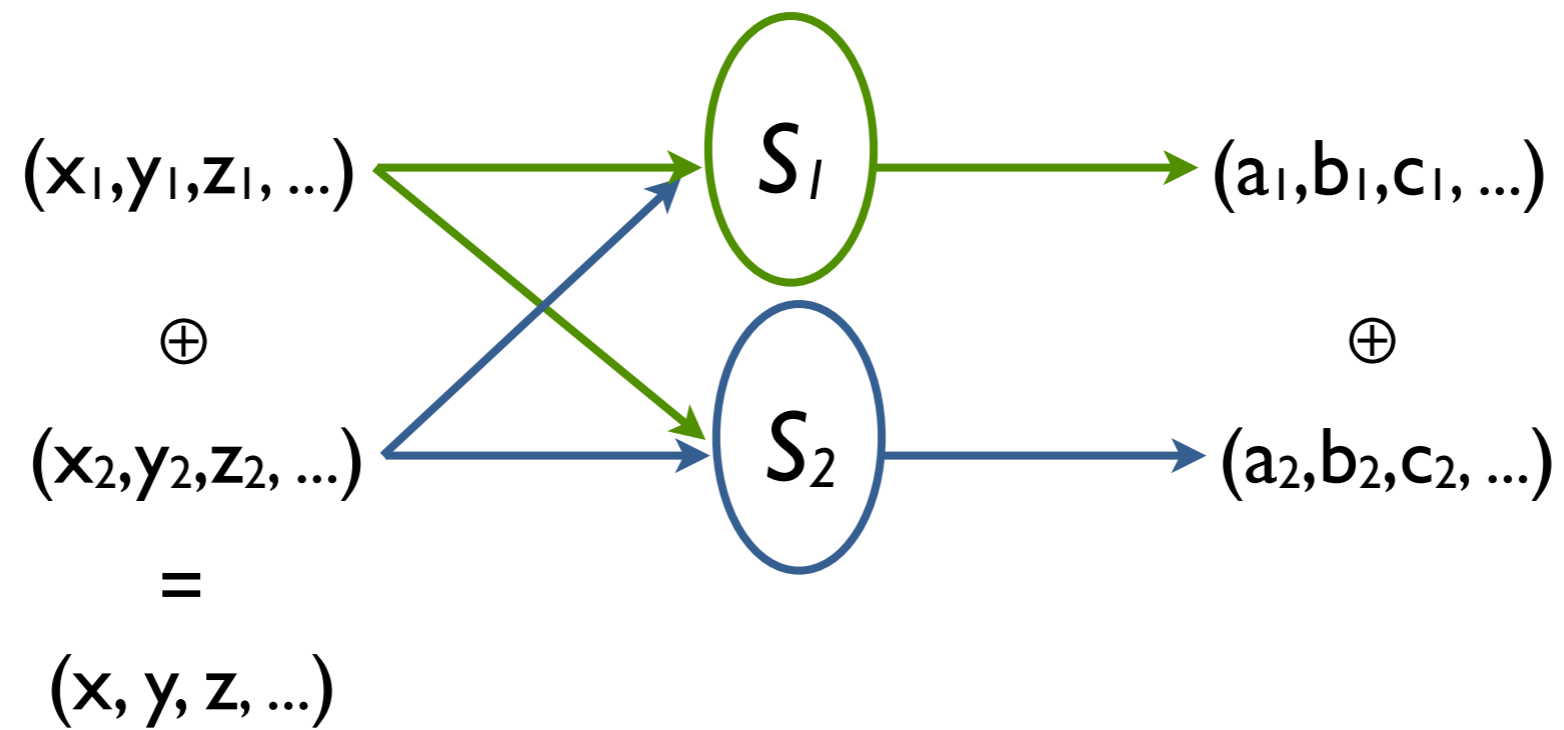
\oplus

(x_2, y_2, z_2, \dots)

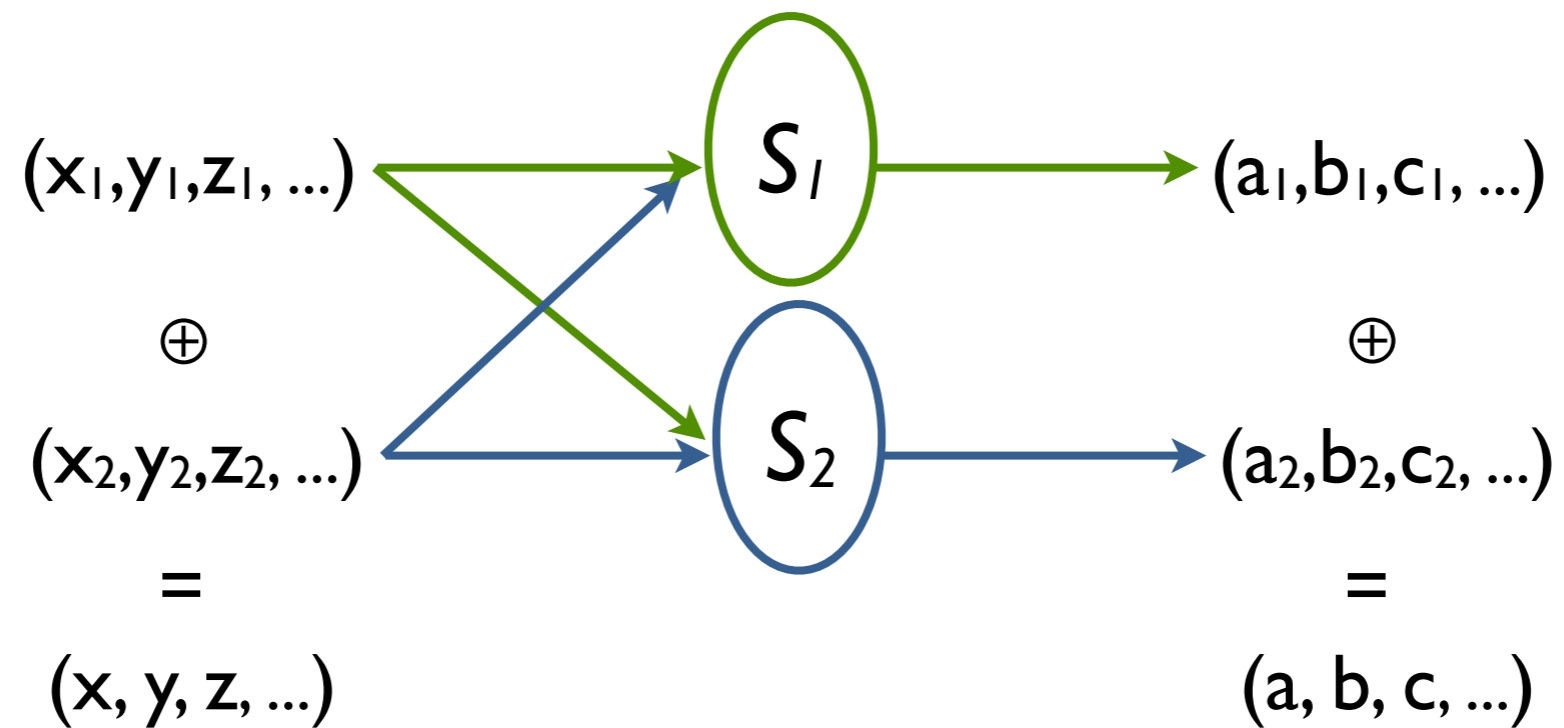
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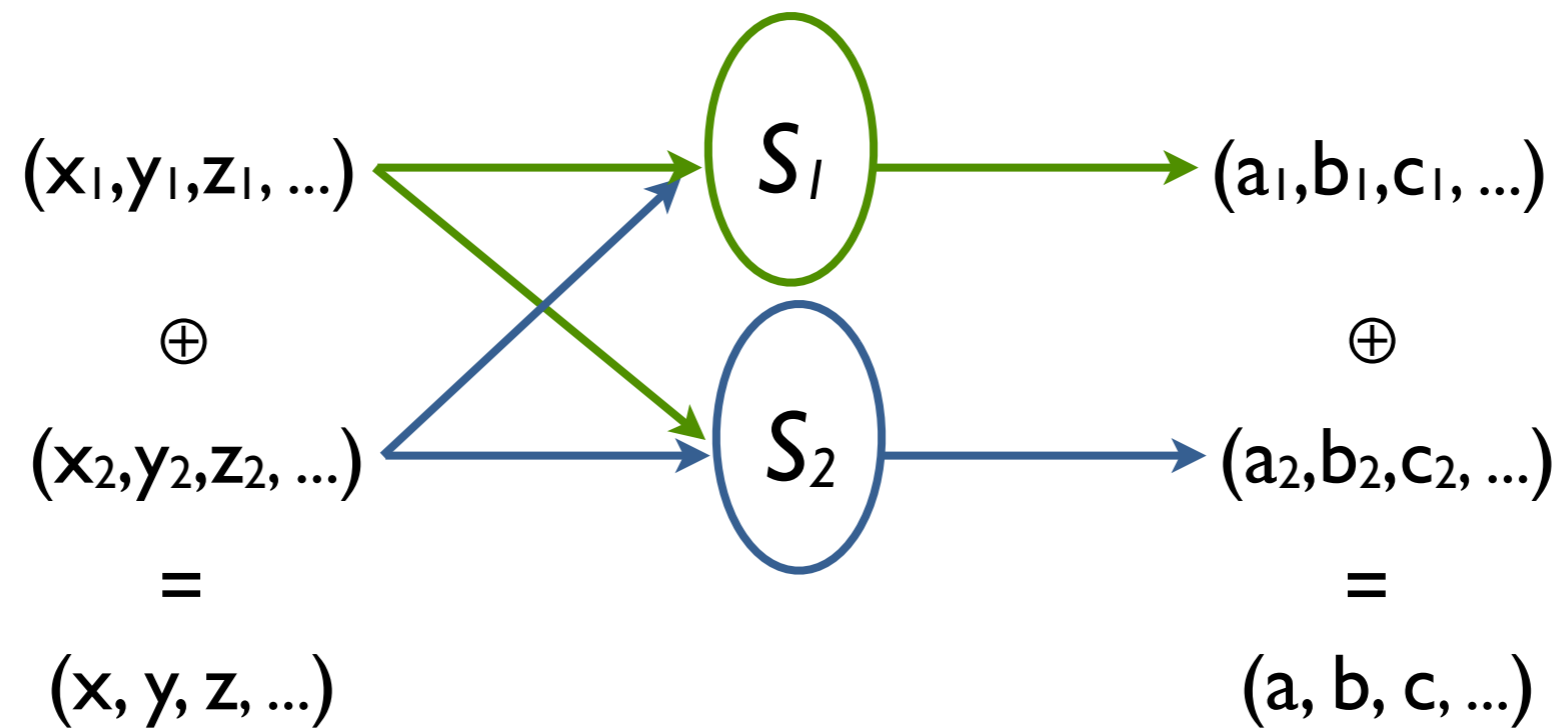
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Random input/output shares \Rightarrow Random intermediate values

Background - Higher-Order DPA

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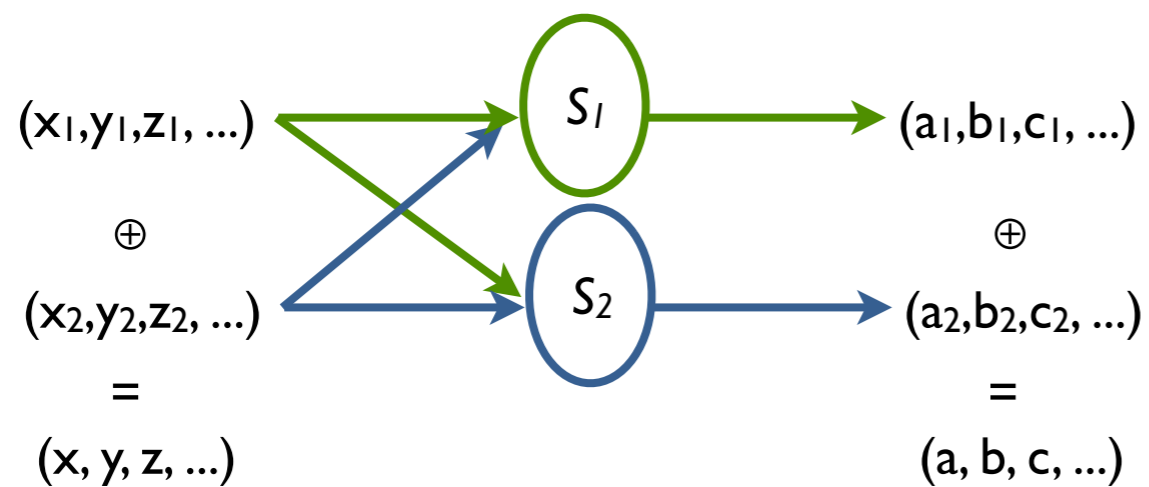
d^{th} -order DPA $\Leftrightarrow d$ probing model

Lemma: Attack order in higher-order DPA corresponds to number of wires probed in the circuit (per unmasked bit).

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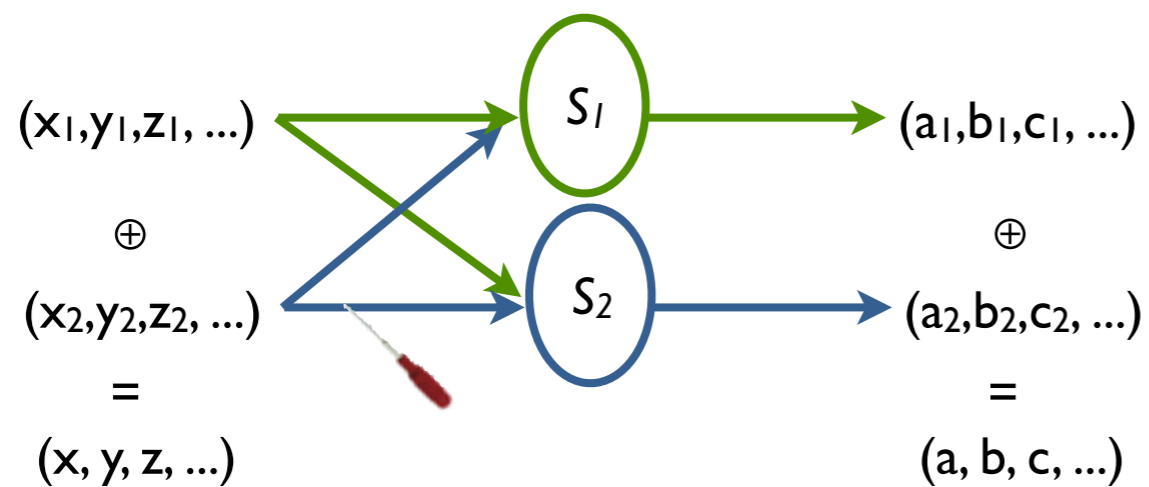
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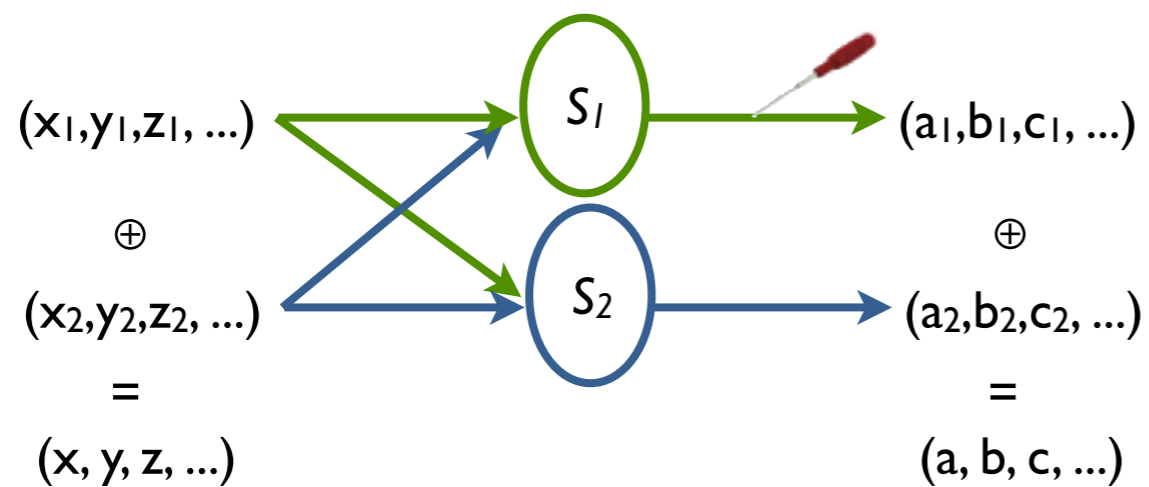
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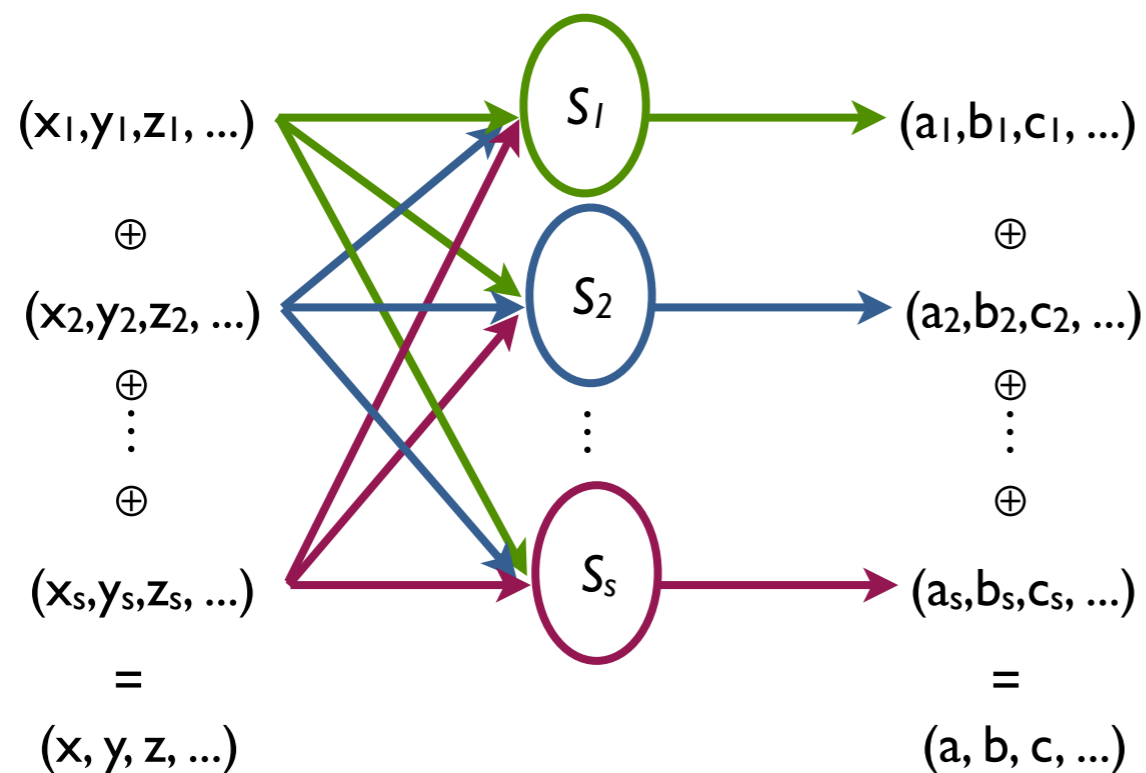
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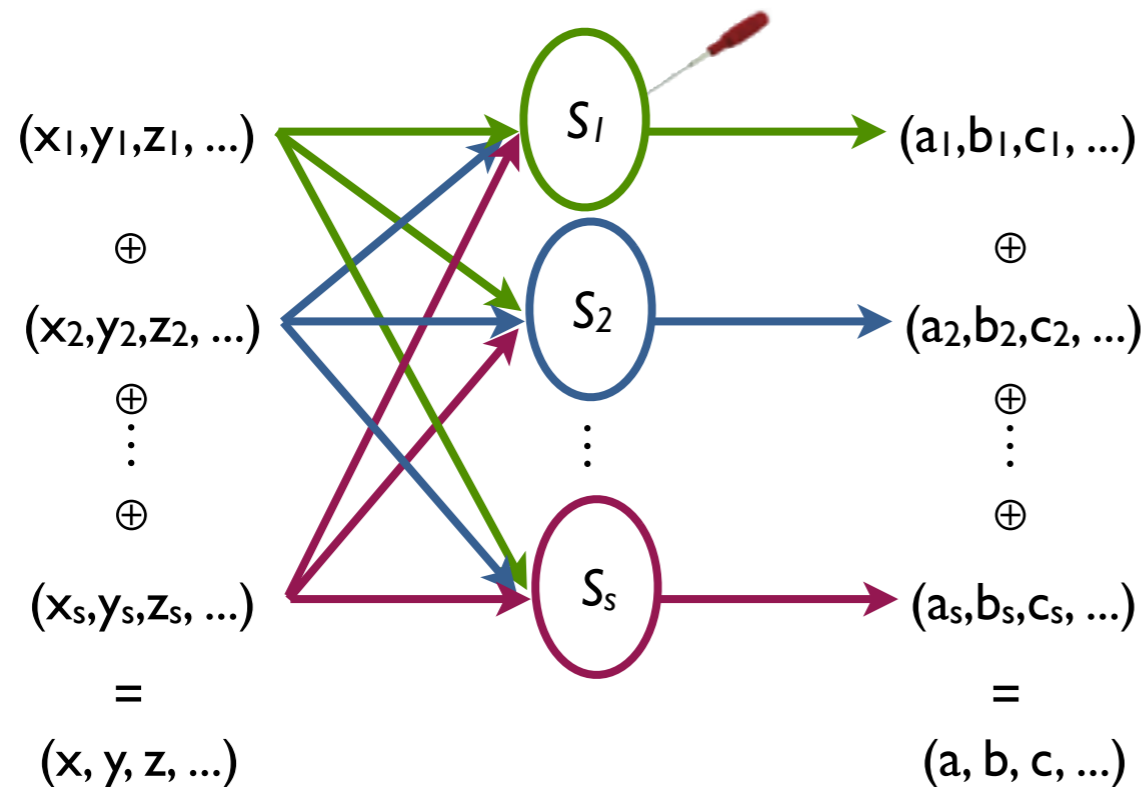
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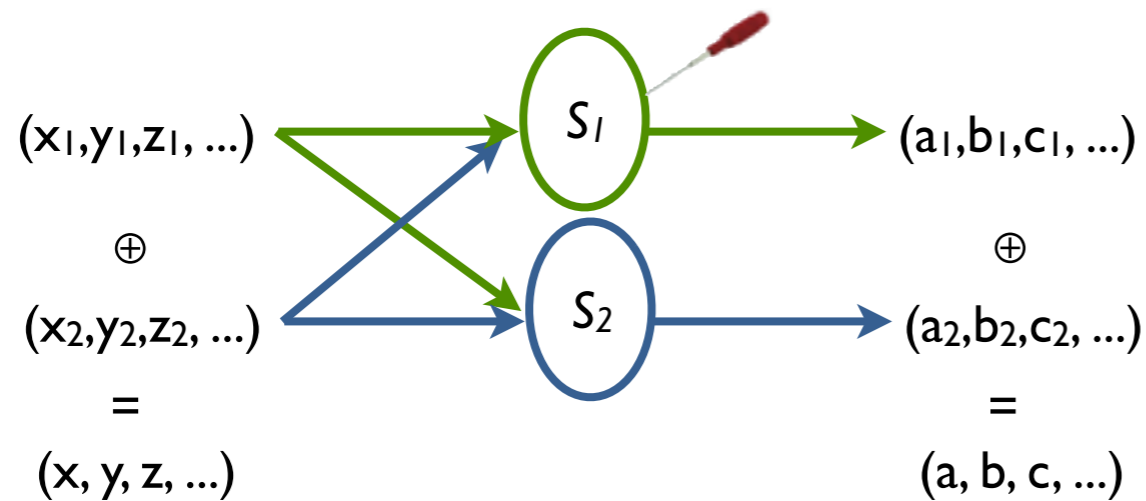
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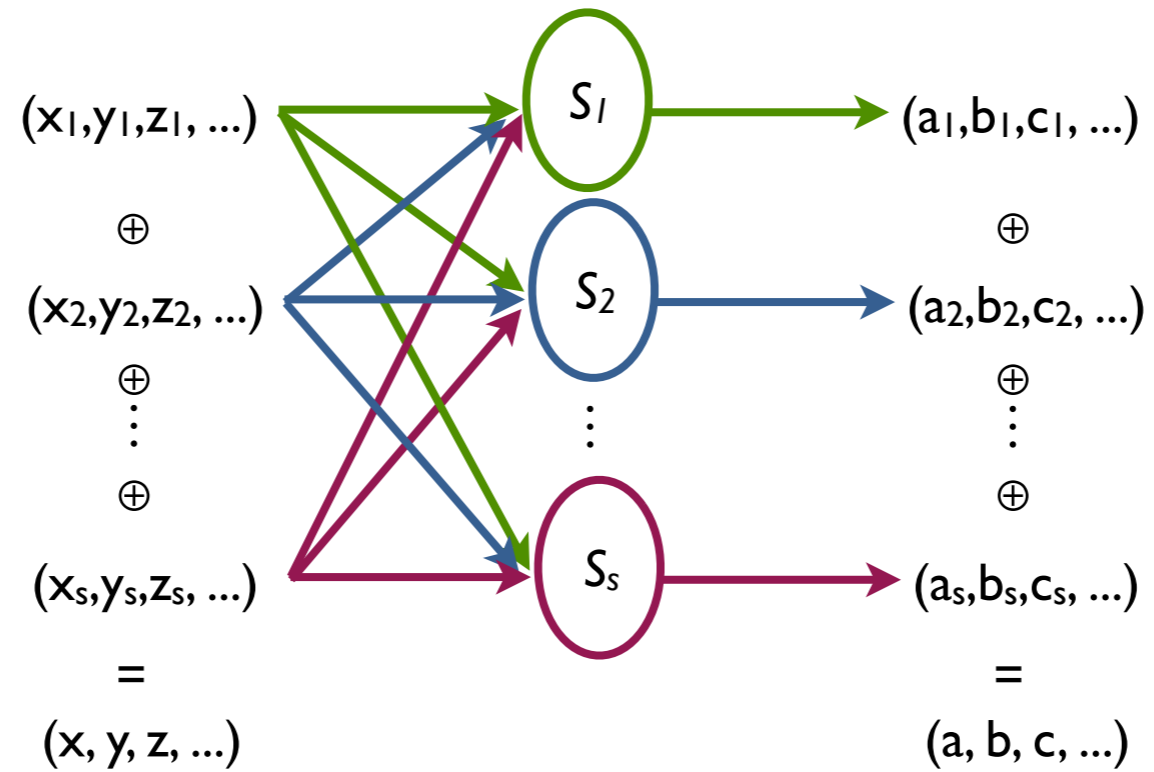
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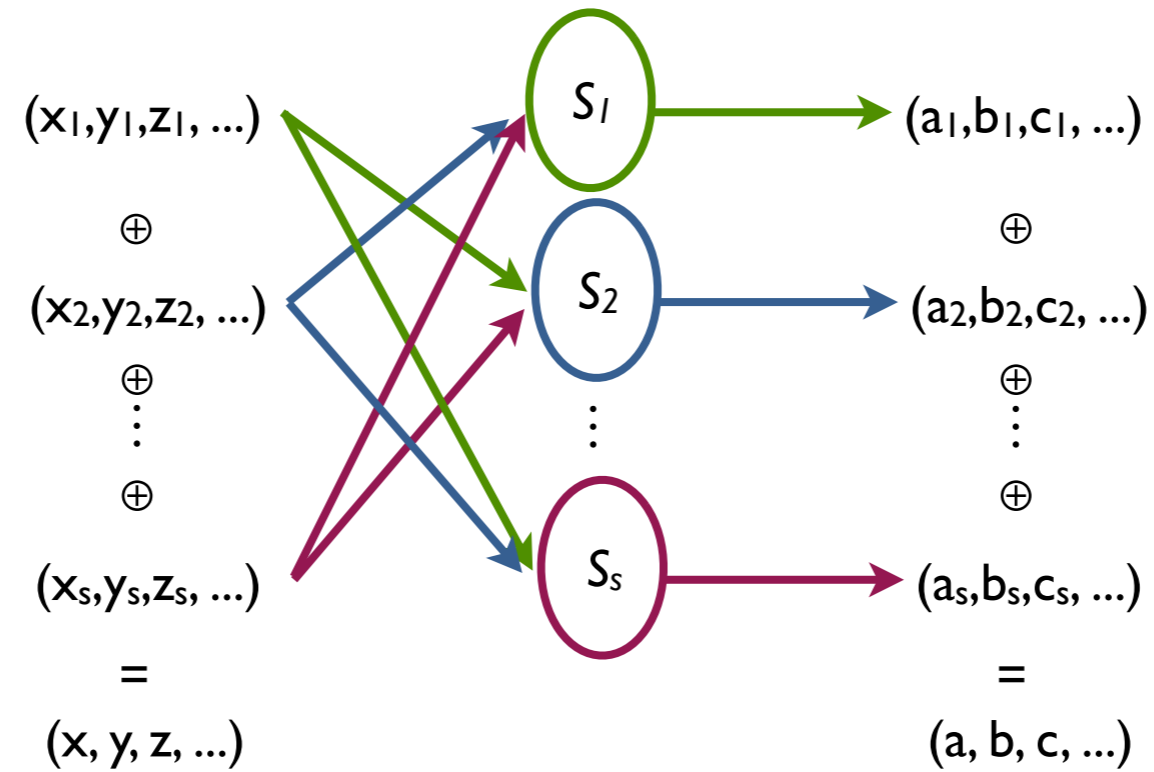
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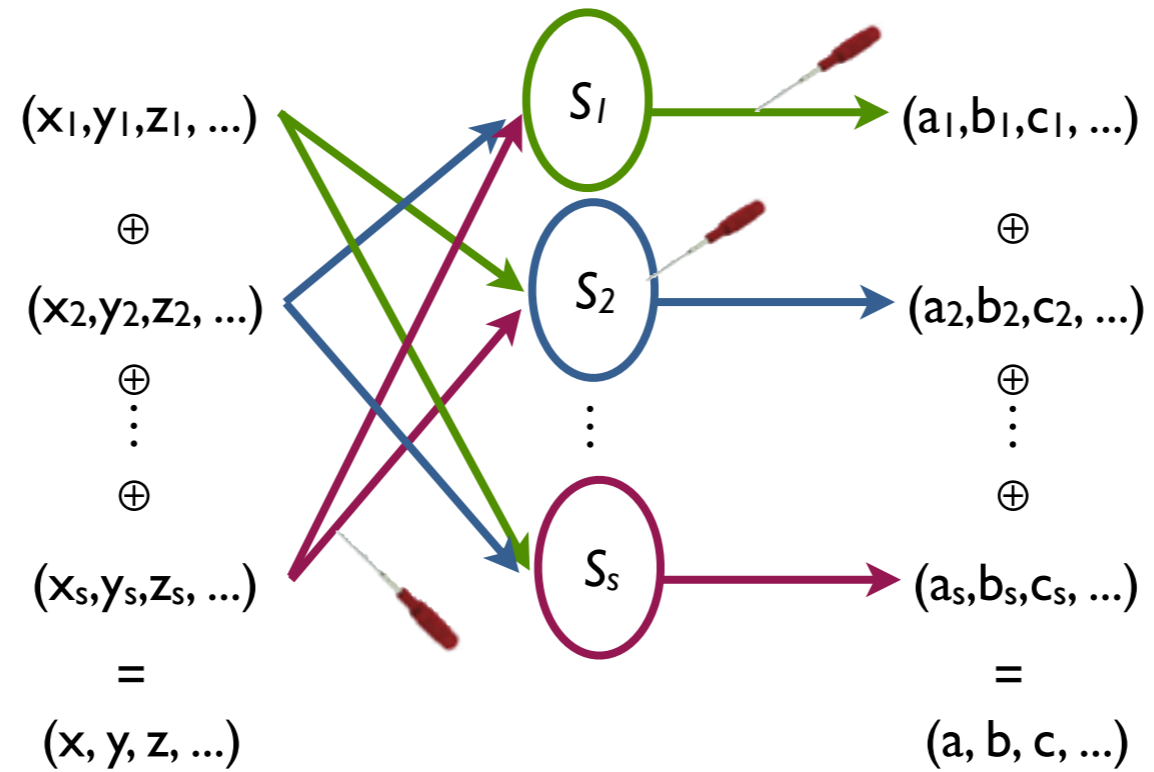
Background - Countermeasures



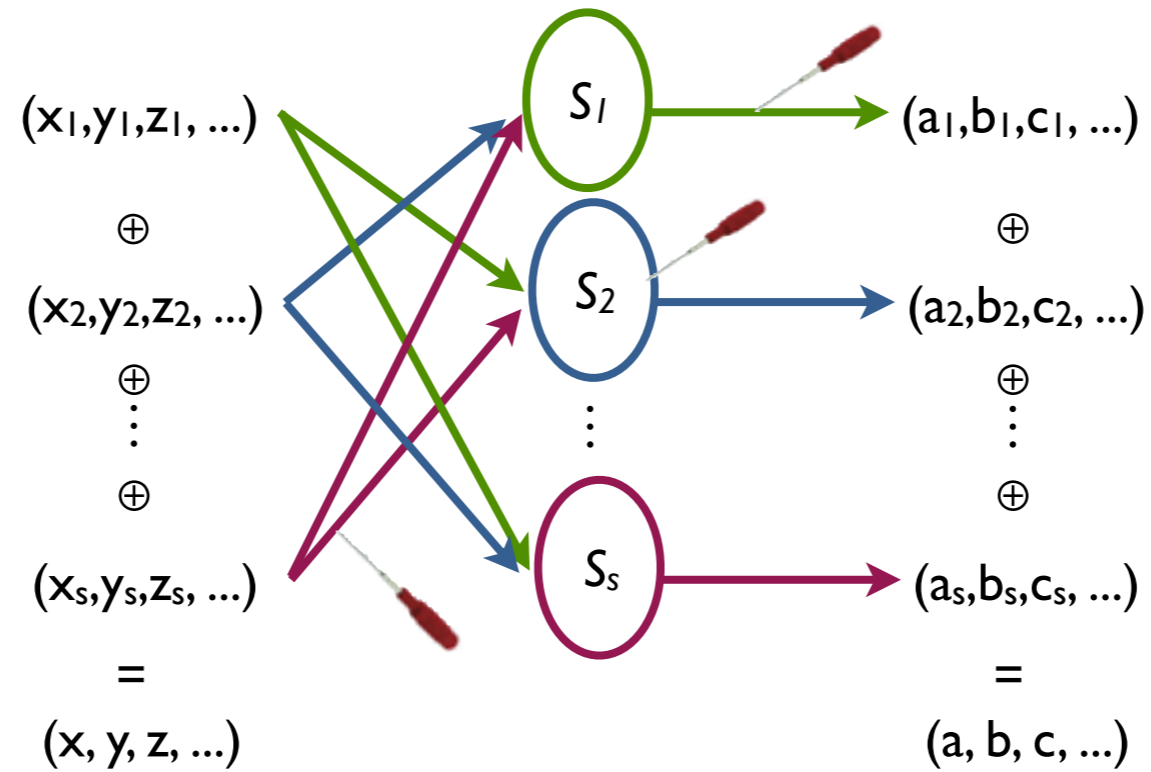
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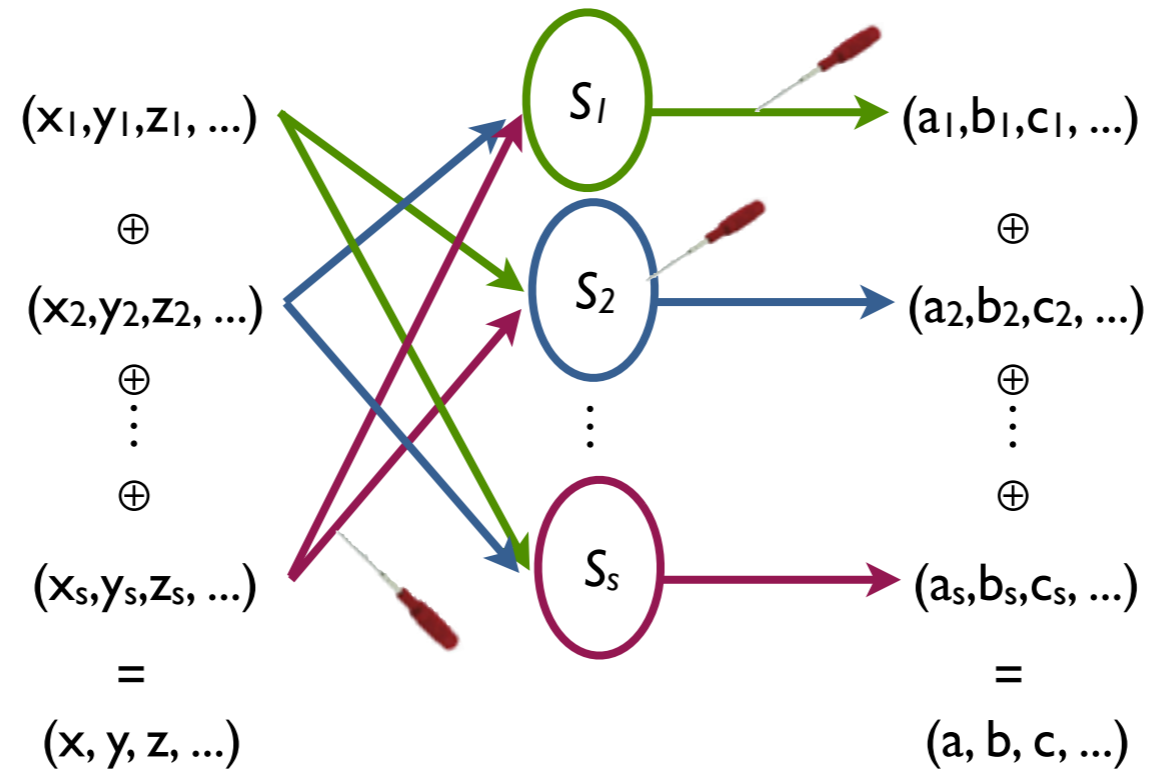


Background - Countermeasures



Such as:

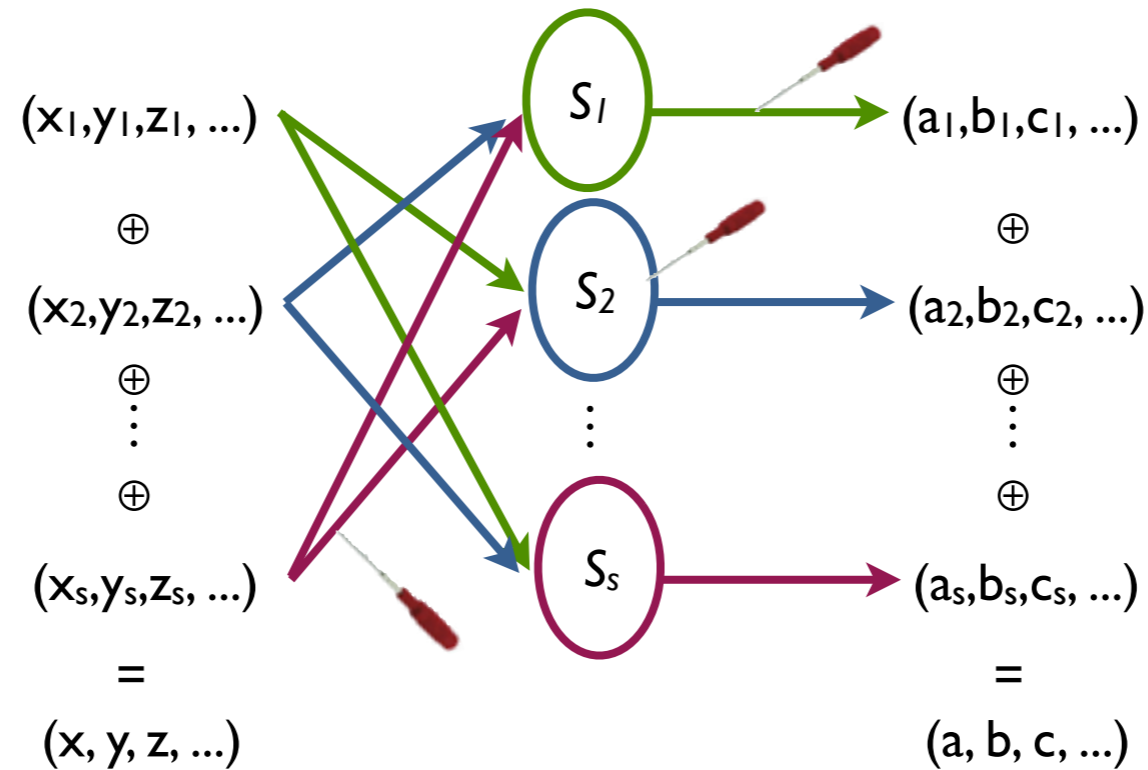
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Such as:

- ($d=1$) Threshold Implementations (ICICS'06)

Background - Countermeasures

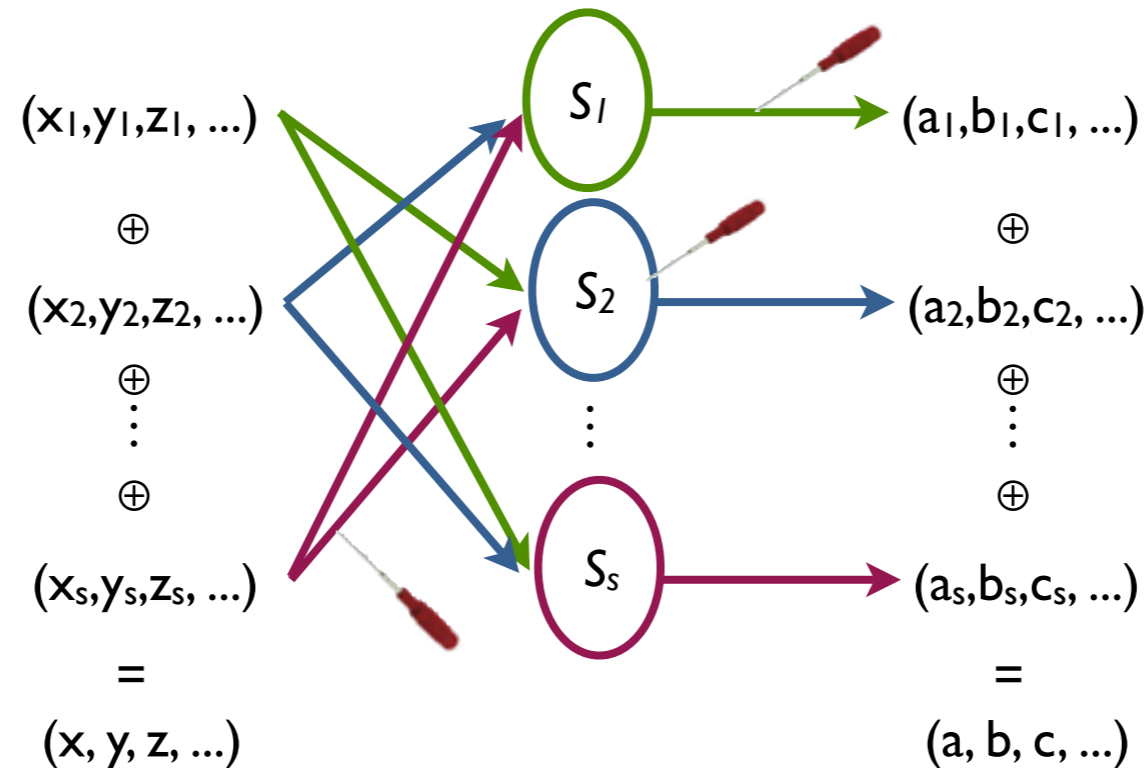


Such as:

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#shares > t (algebraic degree of $S = t$)

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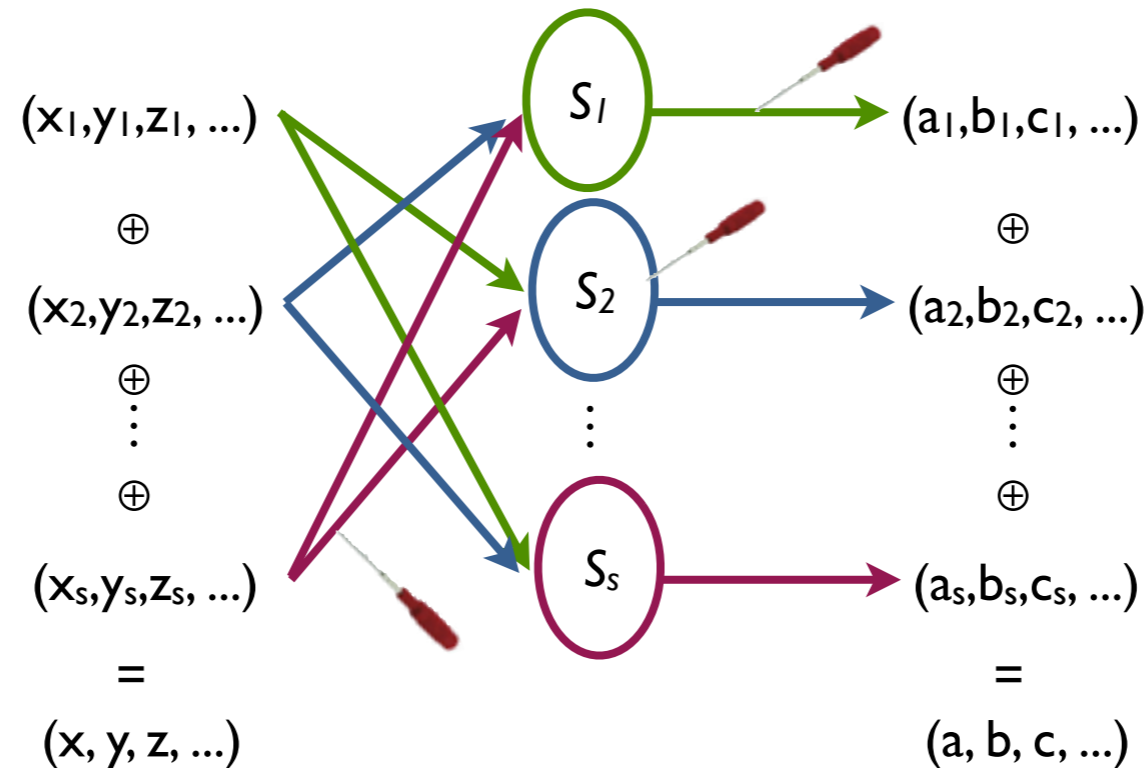
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Background - Countermeasures



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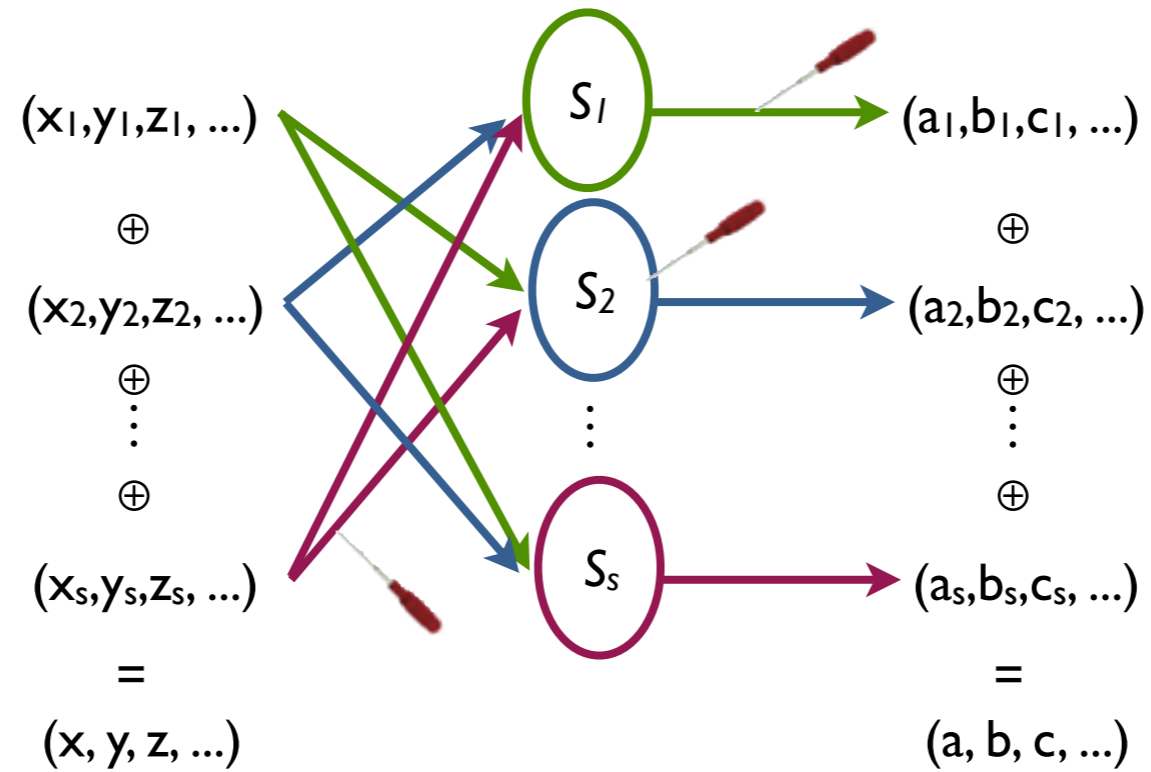
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#shares > 2d

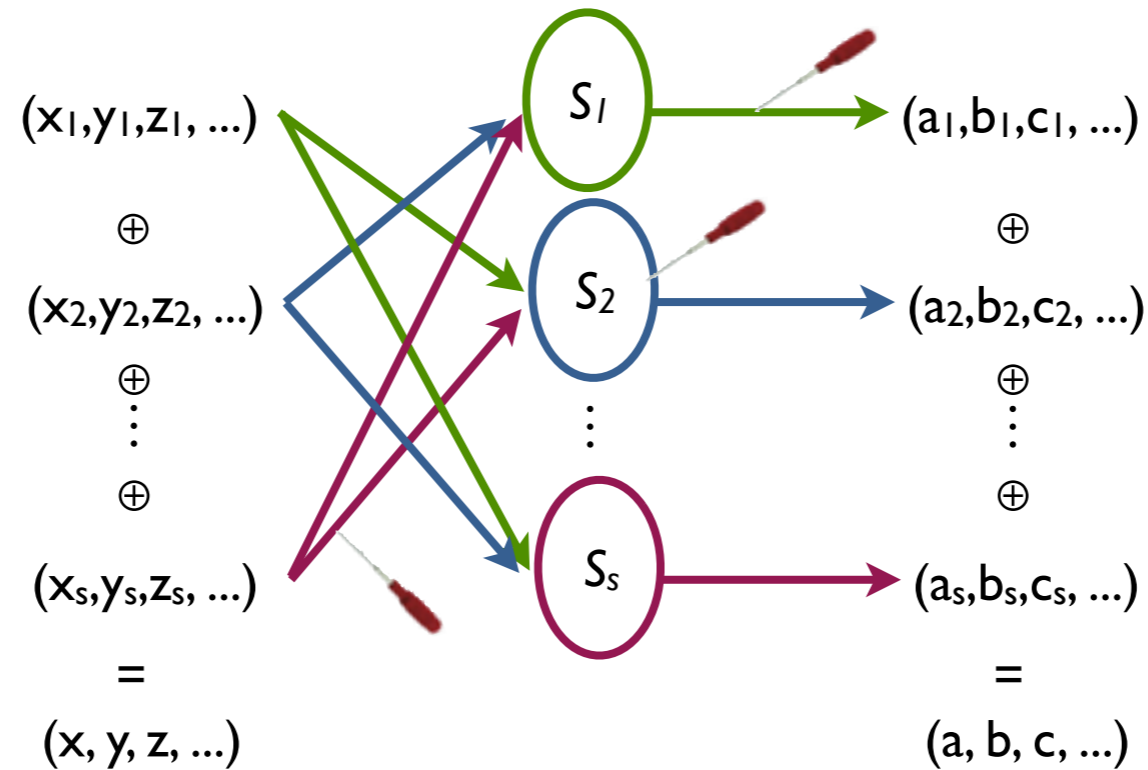
Higher-Order Threshold Implementations

Properties
&
Requirements

Threshold Implementations ($d=1$)



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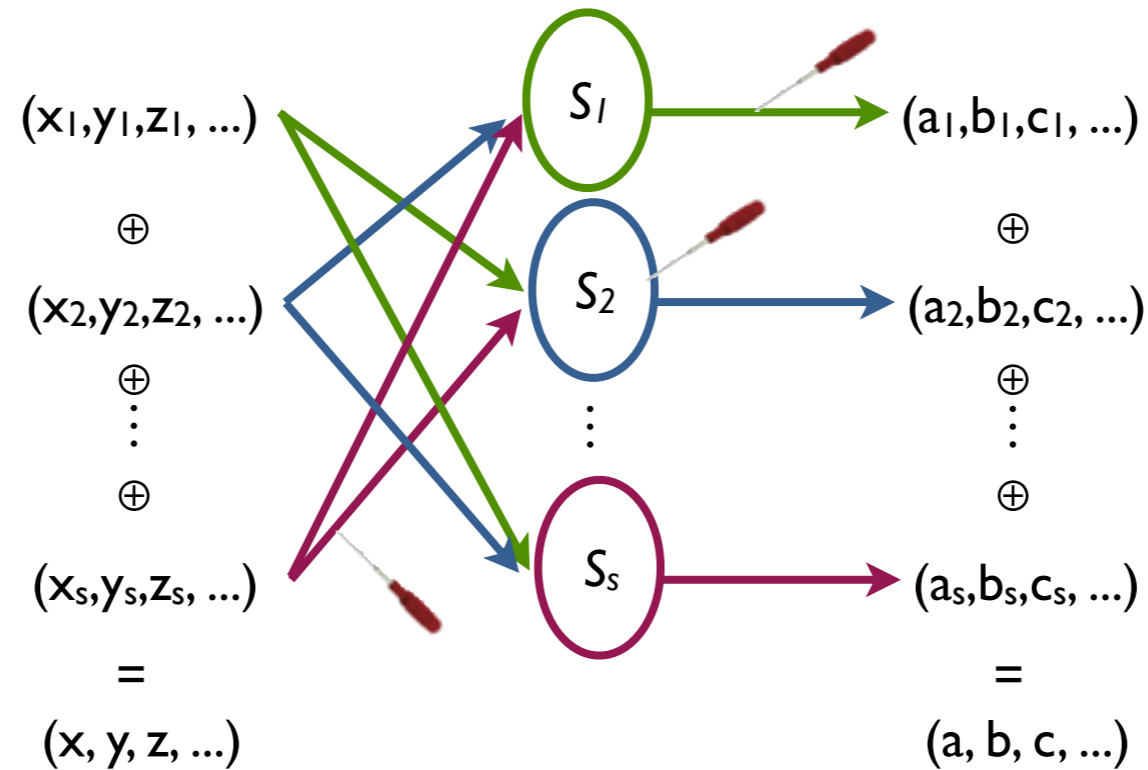


Uniform input masking

Correctness

Non-completeness: Every function is independent of at least one input share.

Higher-Order Threshold Implementations

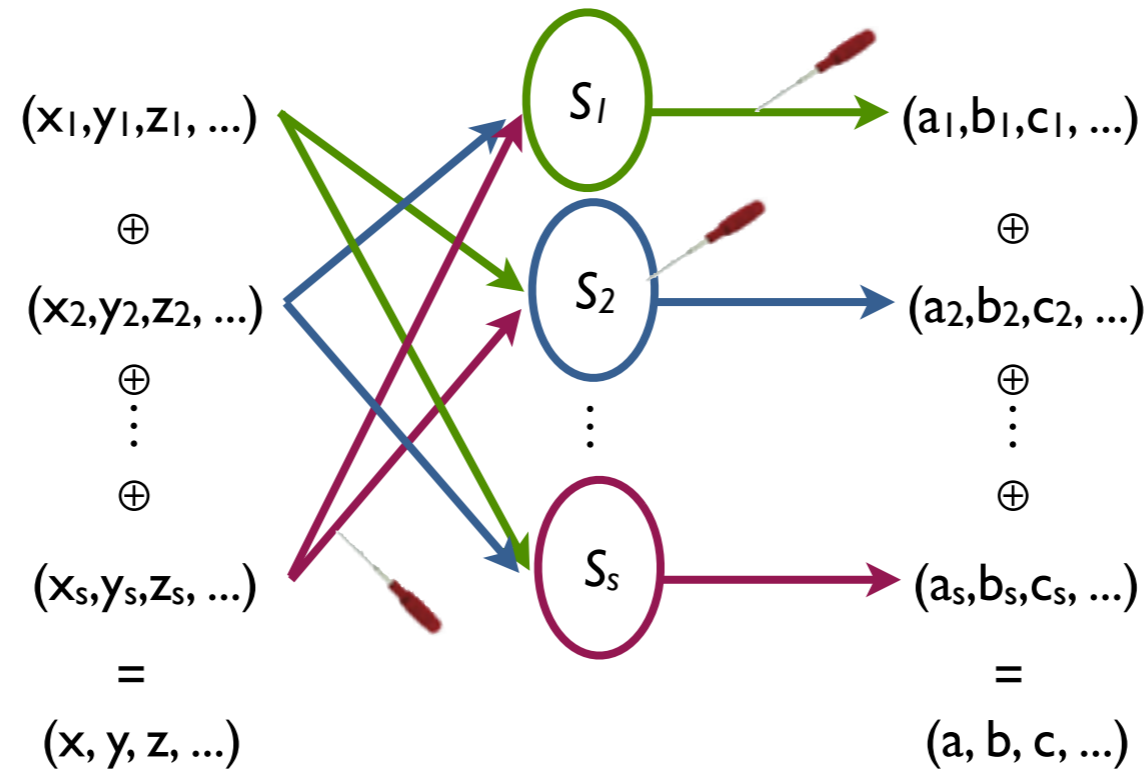


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Higher-Order Threshold Implementations



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How many shares are necessary?

Higher-Order Threshold Implementations

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Linear functions

Higher-Order Threshold Implementations

Linear functions

- $S(x) = S(x_1) \oplus S(x_2) \oplus \dots \oplus S(x_s)$

Higher-Order Threshold Implementations

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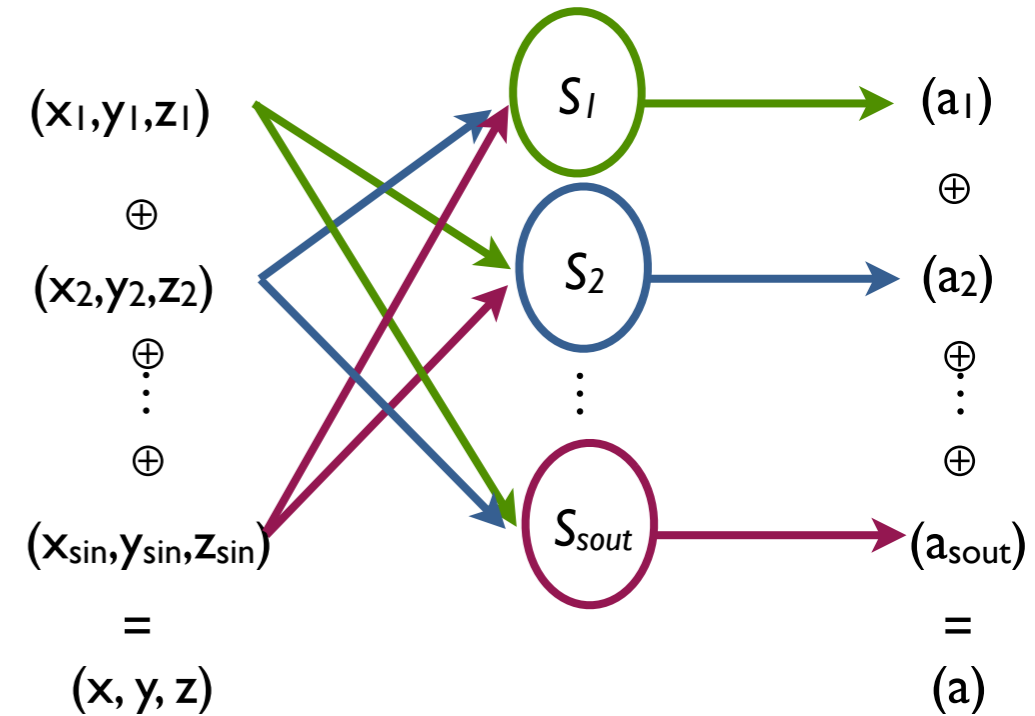
Higher-Order Threshold Implementations

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Nonlinear functions ($a = S(x,y,z) = xy+z$)

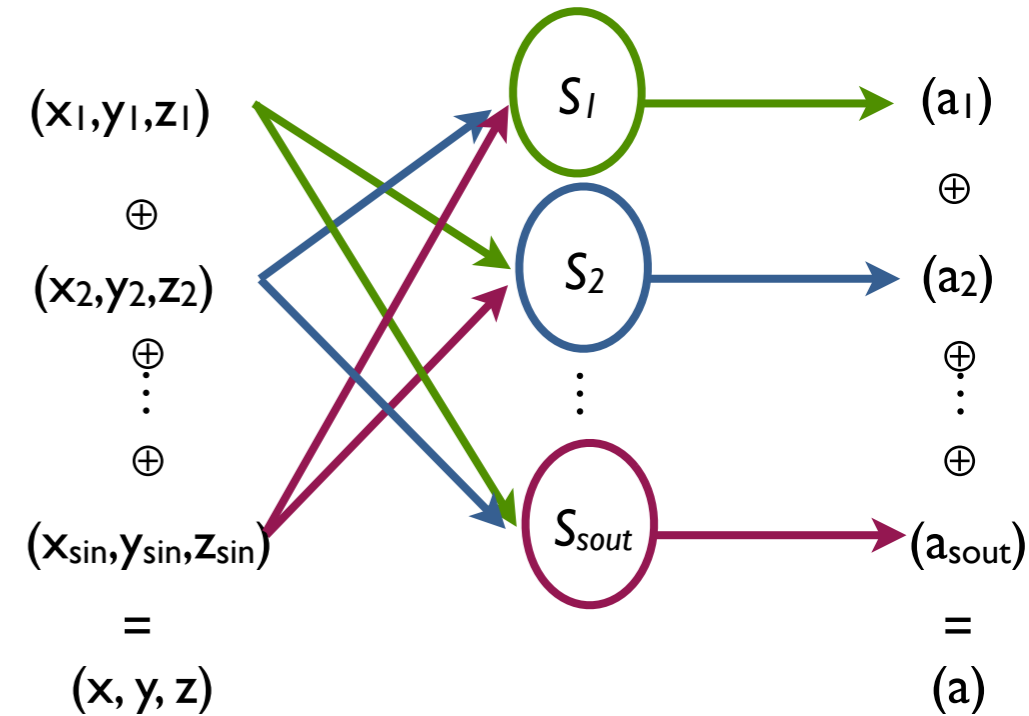
- More challenging



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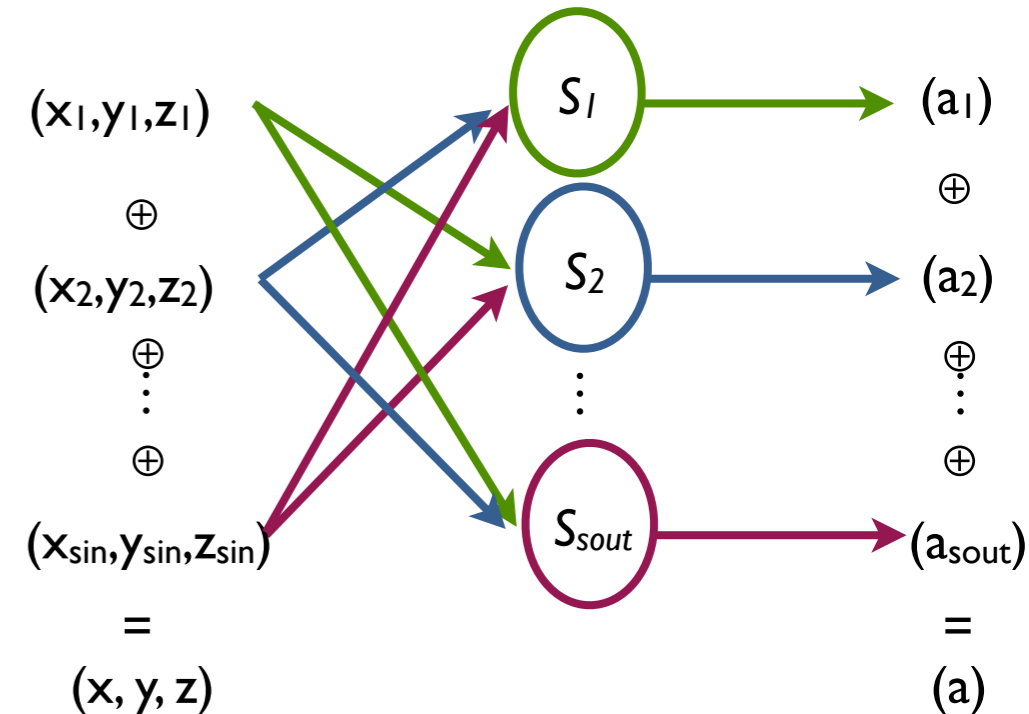
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- More challenging
- $s_{in} \geq td + 1$ and $s_{out} \geq \binom{s_{in}}{t}$ (algebraic degree of $S = t$)

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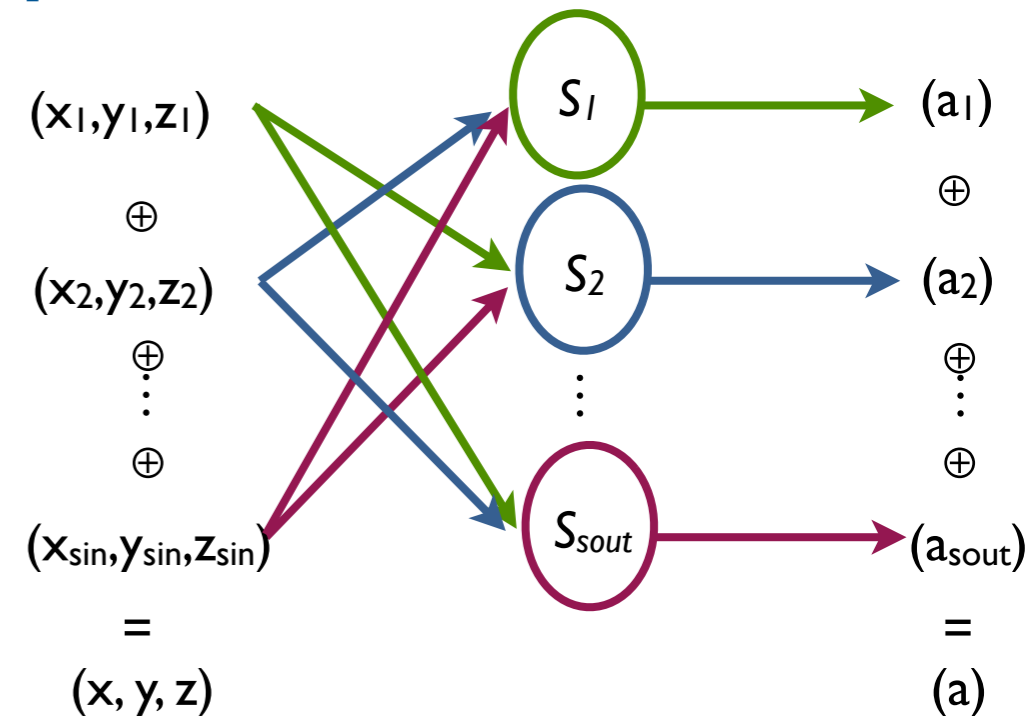
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- First-order $s_{in} \geq 3$ input $s_{out} \geq 3$ output shares
- Second-order $s_{in} \geq 5$ input and $s_{out} \geq 10$ output shares

Higher-Order Threshold Implementations

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Two issues to solve in the system:

Higher-Order Threshold Implementations

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1. Increase of the number of shares when $d > 1$

Higher-Order Threshold Implementations

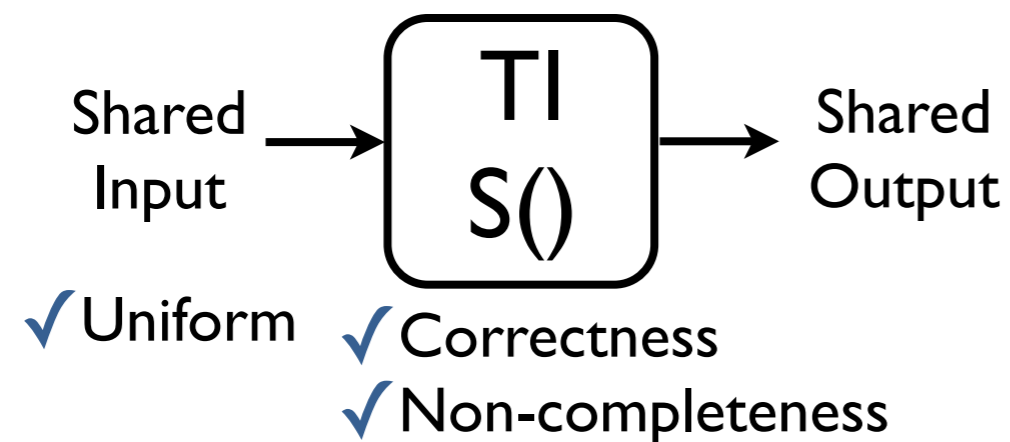
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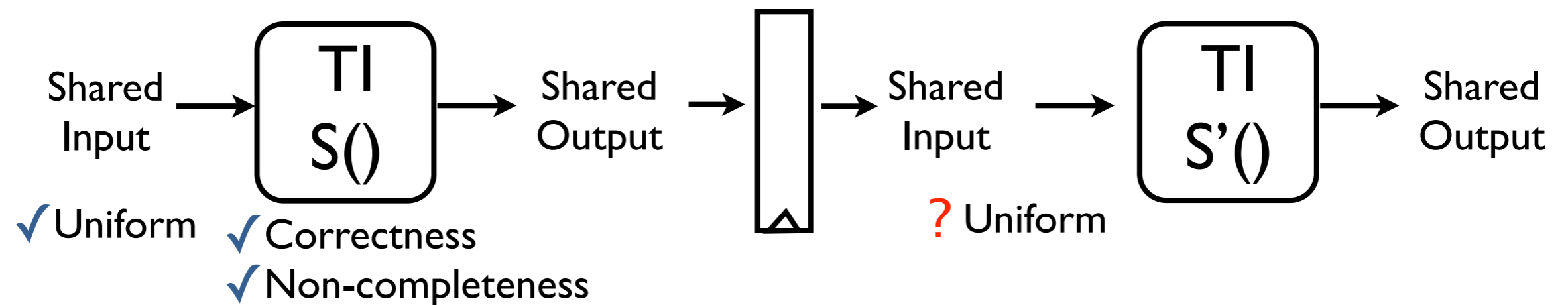
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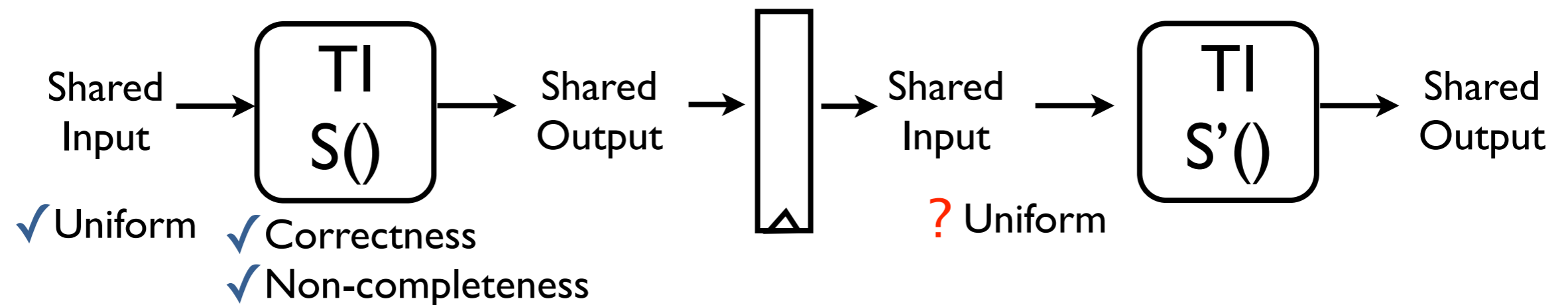
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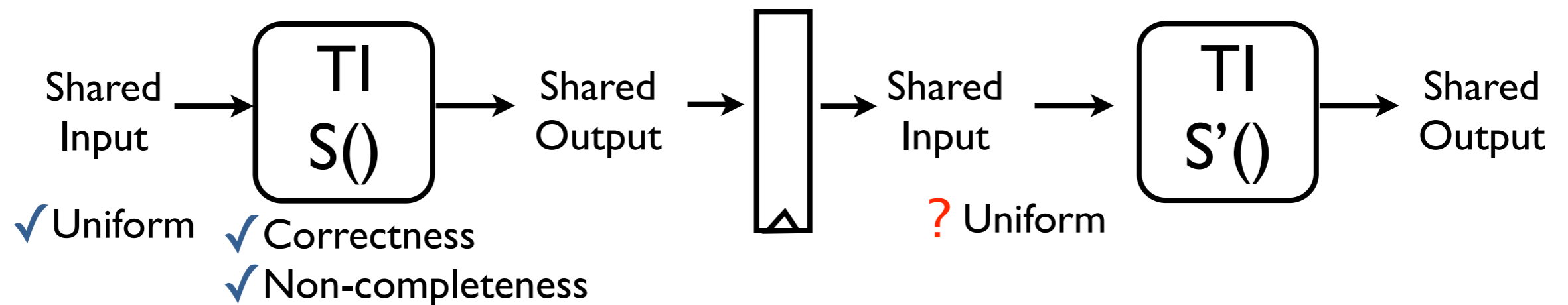


One solution: XOR some of the output shares

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One solution: XOR some of the output shares

In our paper:

- Uniform HO-TI of an AND/XOR gate
- Uniform second-order TI of quadratic 4-bit permutations

Higher-Order Threshold Implementations

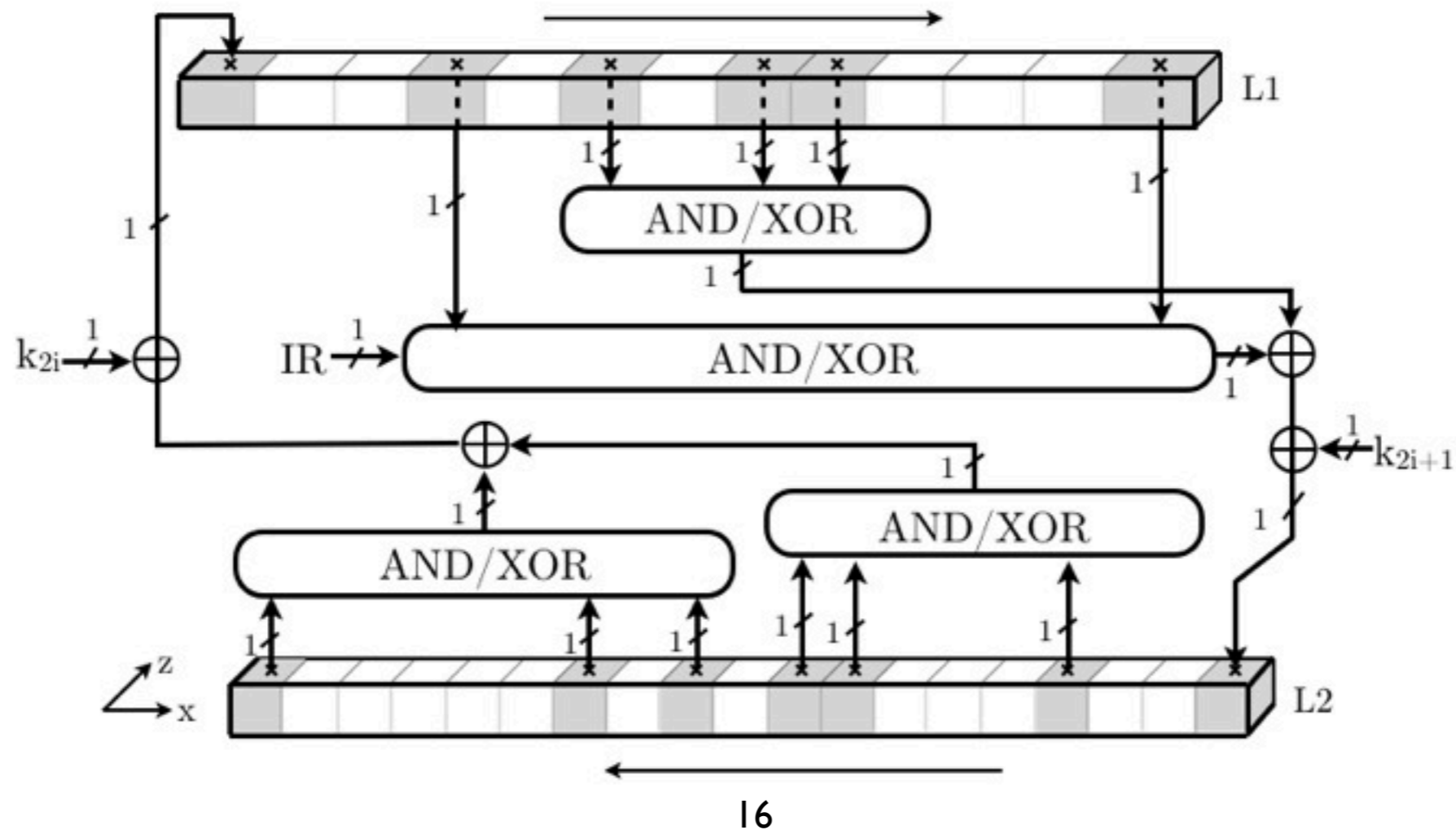
Application to a cryptographic algorithm
&
Testing

Higher-Order Threshold Implementations

Second-order TI of KATAN-32
&
Leakage Detection Tests on SASEBO-G

KATAN-32

- 254-round block cipher
- 32-bit plain/cipher-text and 80-bit key
- Round keys are generated by an LFSR



HO-TI of KATAN-32

Linear: $s \geq d+1$

Nonlinear: $s_{in} \geq td+1$ and $s_{out} \geq \binom{s_{in}}{t}$

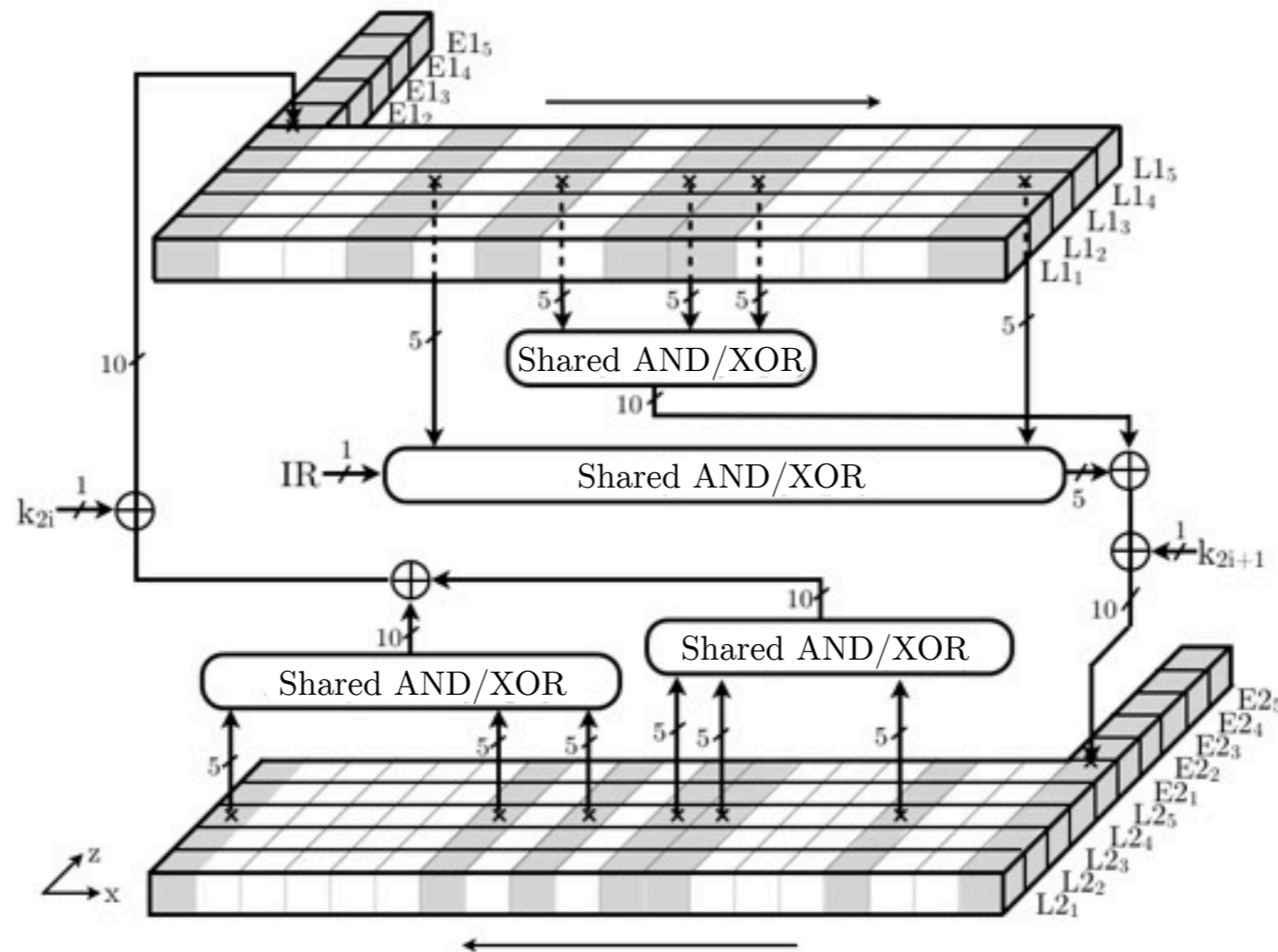
	# of shares		
	Linear	Nonlinear	
		s_{in}	s_{out}
Unprotected	1	1	1
First-Order TI	3	3	3
Second-Order TI	5	5	10
Third-Order TI	7	7	21

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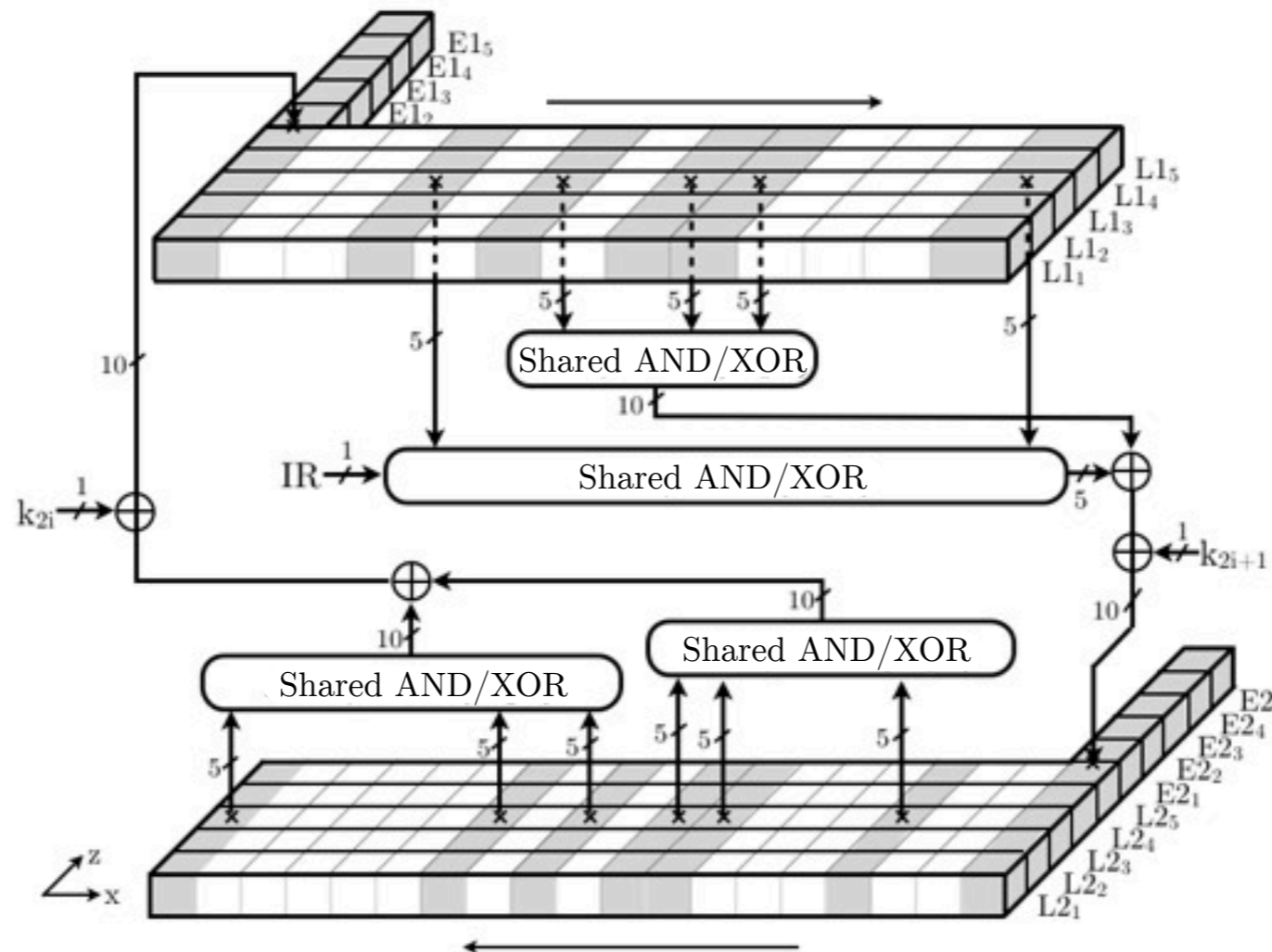


HO-TI of KATAN-32

Linear: $s \geq d+1$

Nonlinear: $s_{in} \geq td+1$ and $s_{out} \geq \binom{s_{in}}{t}$

	# of shares			Area (GE) Faraday Standard Cell Library FSA0A C Generic Core
	Linear	Nonlinear		
		s_{in}	s_{out}	
Unprotected	1	1	1	1002
First-Order TI	3	3	3	1720
Second-Order TI	5	5	10	2556
Third-Order TI	7	7	21	3539



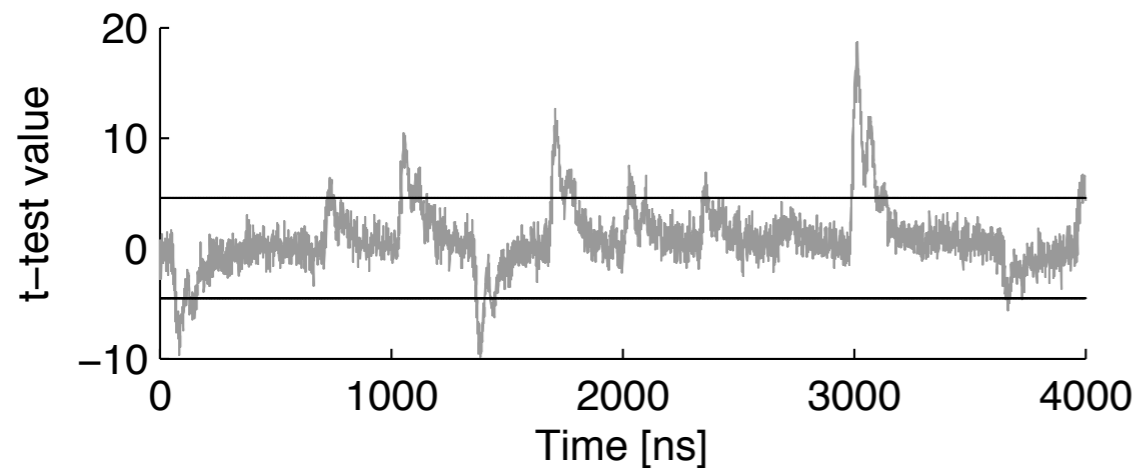
HO-TI of KATAN-32 - Analysis

Fix vs. random leakage detection test
RNG is OFF to test the setup

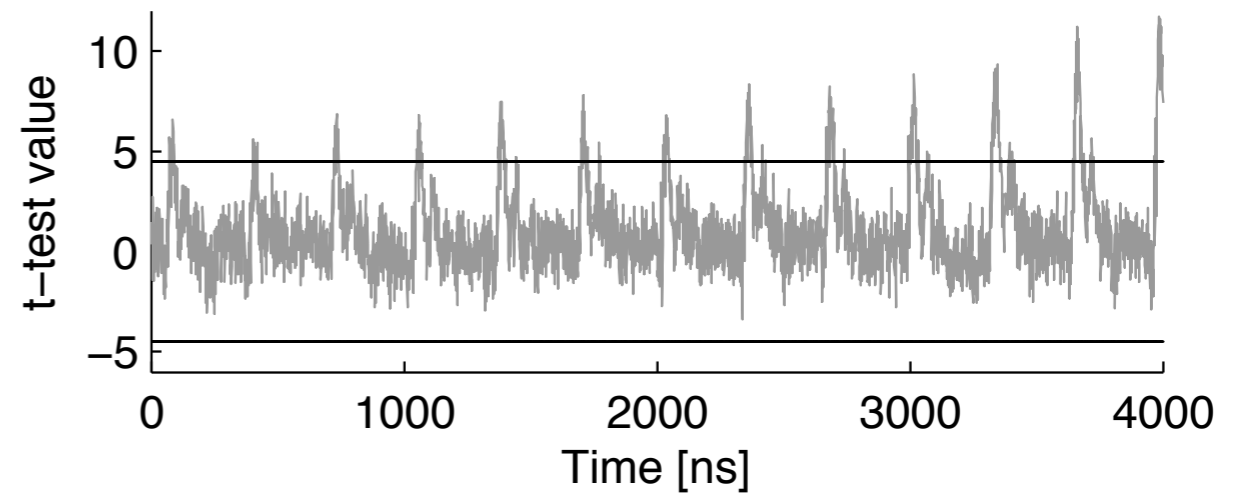
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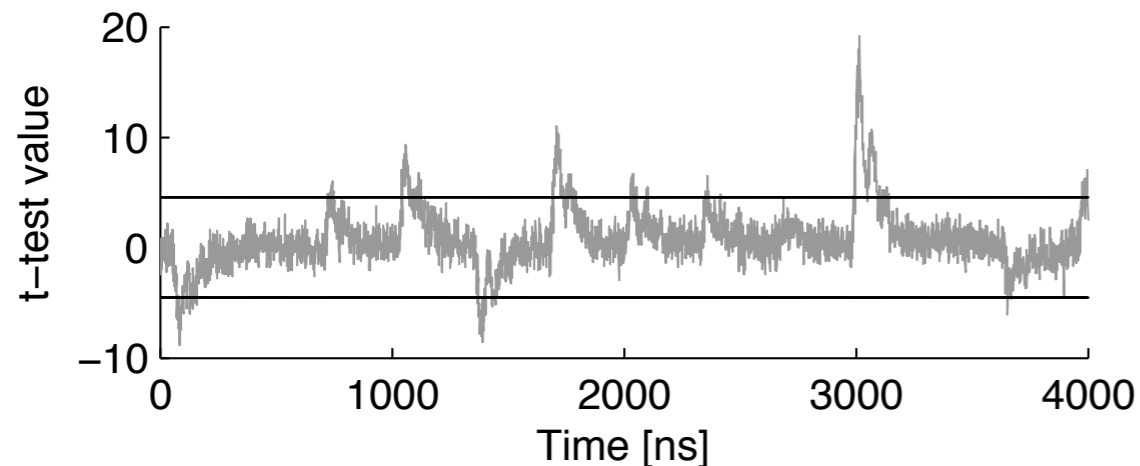
1st-order



2nd-order



3rd-order



HO-TI of KATAN-32 - Analysis

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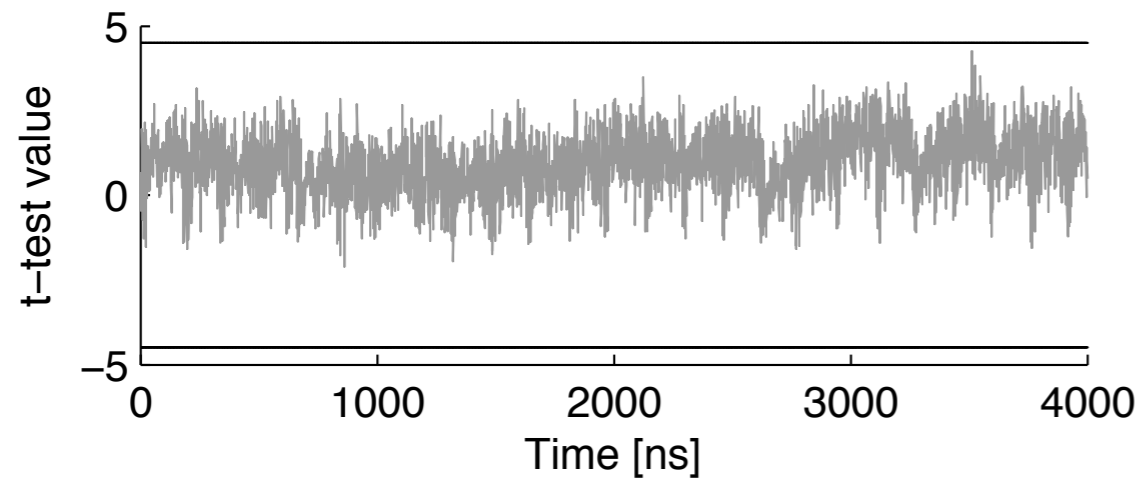
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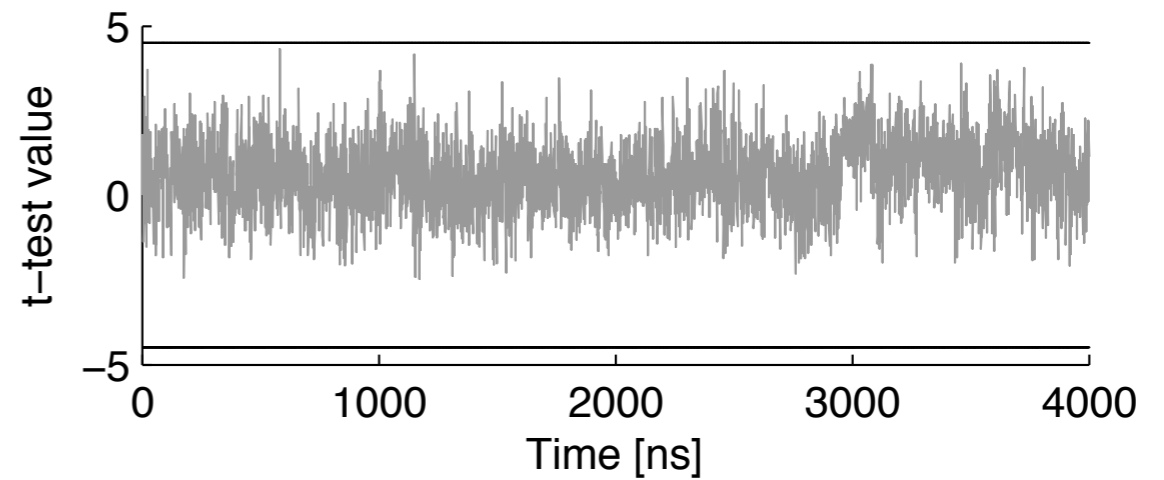
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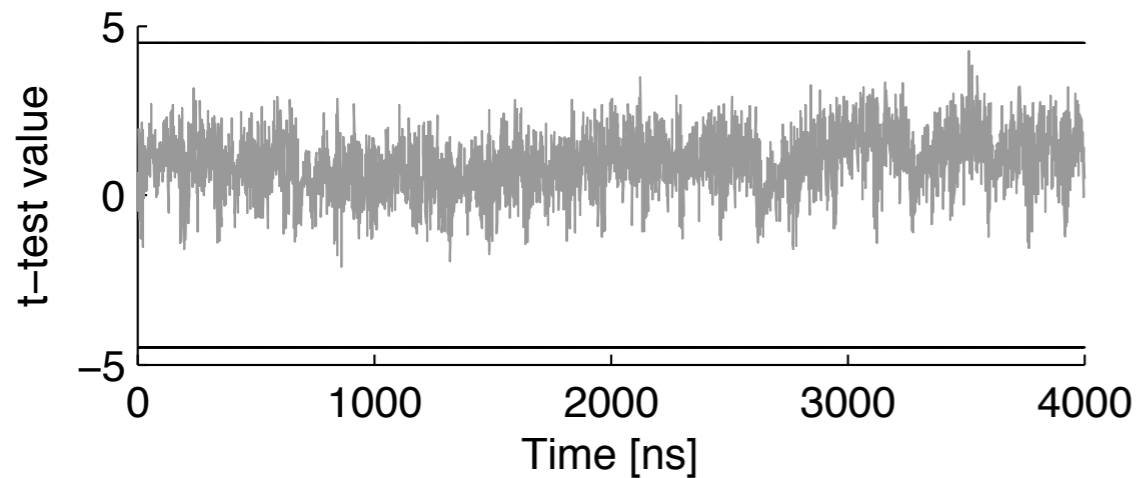


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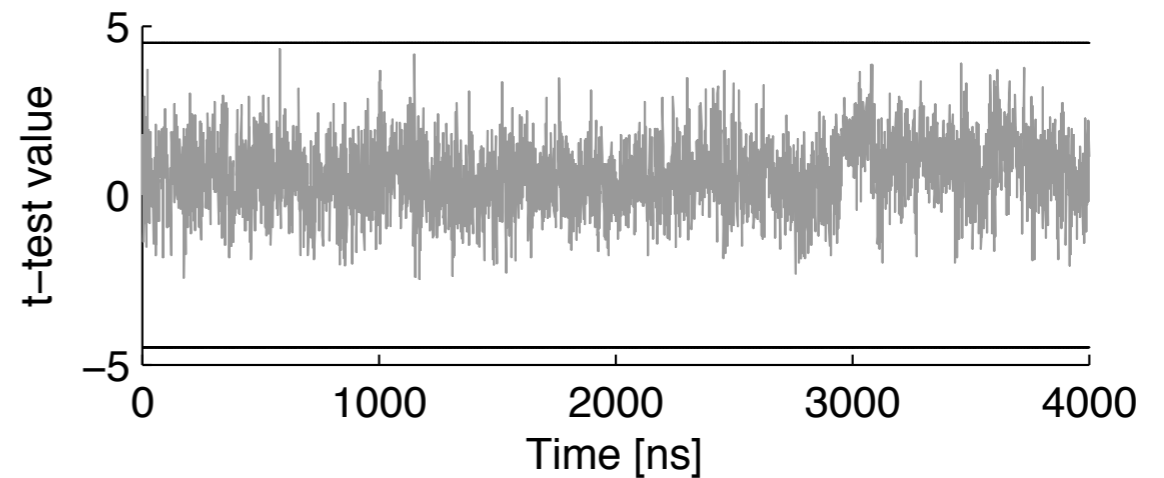
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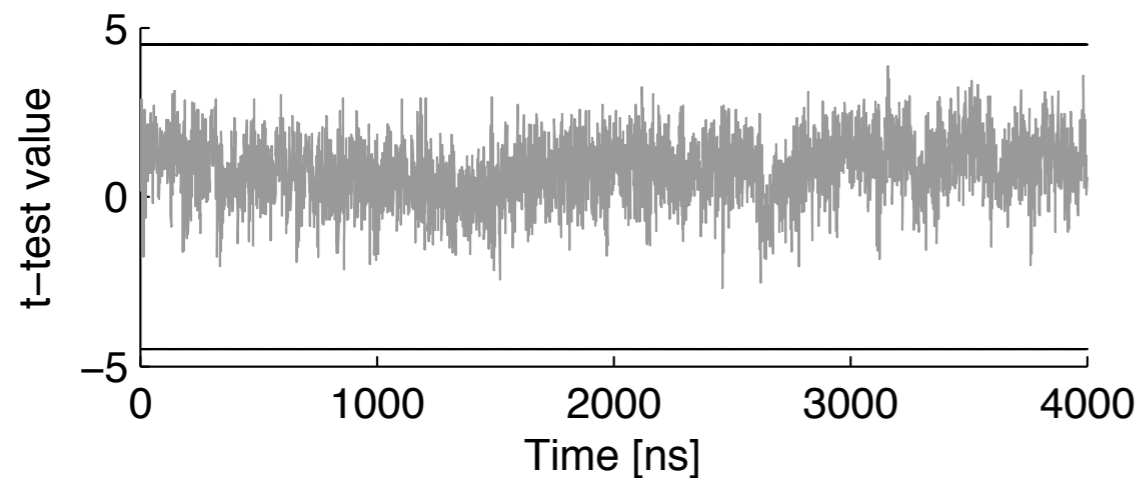
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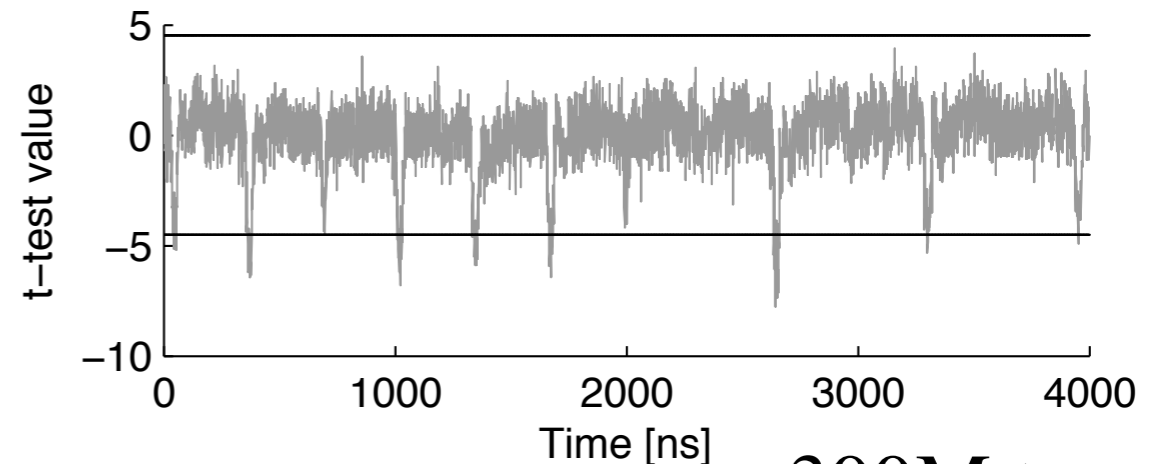
2nd-order



3rd-order



5th-order



Conclusion

- Countermeasure against HO-DPA
- Efficient TIs of KATAN-32
- Confirmed the claimed security using leakage detection tests
- Methods for second-order TI of quadratic 4-bit permutations

Thank You!

